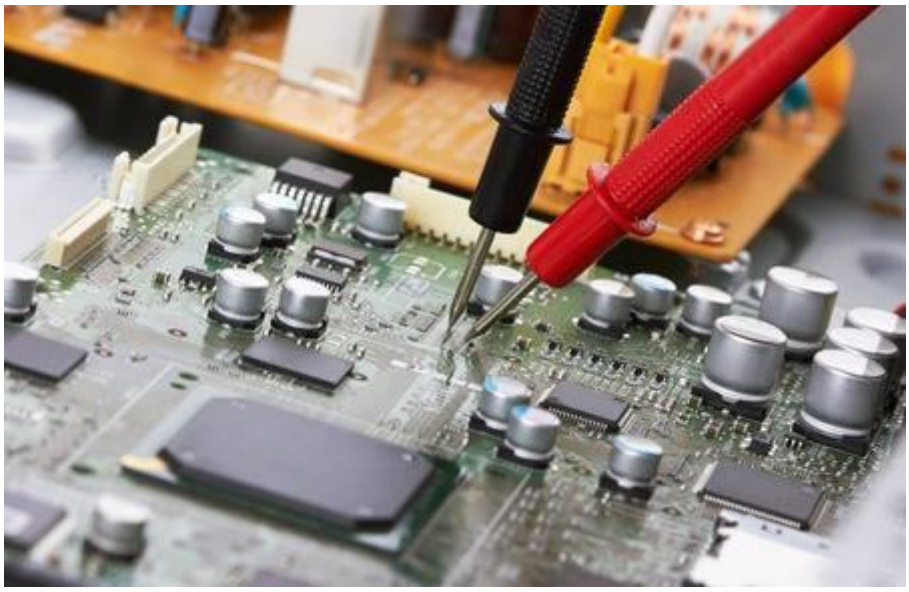
كلية الهندسة
جامعة الملك سعود
King Saud University
College Of Engineering

EE 312

Laboratory Manual



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OBJECTIVES

- Introducing the students to the basic electronic devices, their applications, and some aspects of their limitations
- Exposing the students to laboratory instruments and modern engineering tools
- Building the students' circuit design and construction skills
- Developing the students technical writing skills

EVALUATION AND GRADING POLICY

Attendance and Skills Assessment	15%
Reports	10%
Assignments	10%
Midterm Exam	25%
Final Exam Part I (Design and Simulation)	10%
Final Exam Part II	30%

EE312 Website**:** http://fac.ksu.edu.sa/talmadhi/course/157758

QR code to lab manual in pdf format:

Course Schedule

Week No.	Activity	Notes
1	Experiment 1	
2	Experiment 2	Submit Assignment 1
3	Experiment 3	Submit a report for (Exp. 2)
4	Experiment 4	Submit Assignment 2 Submit Assignment 3
5	Experiment 5	Submit a report for (Exp. 3)
6	Revision	Submit Assignment 4
7	Midterm Exam	Submit a report for (Exp. 4)
9	Experiment 6	
10	Experiment 7	Submit Assignment 5
11	Experiment 8	Submit a report for (Exp. 7)
12	Experiment 9	Submit Assignment 6
13	Experiment 10	Submit Assignment 7
15	Design and Simulation Quiz + Revision	
16	**Final Exam**	

Guidelines for Writing EE 312 Reports

Your reports should be computer-typed and spell-checked. Paragraphs should be written in Times New Roman, size 12 points. Headings should be in upper case, bolded and size 14 points. Use formal English, direct language, and simple terms. The following link has good information that might help you to improve your technical writing skills.

https://msu.edu/course/be/485/bewritingguideV2.0.pdf

Use the following checklist to complete the requirements for each experiment you are asked to submit a report for (see the previous page).

Your reports/assignments should be uploaded via LMS: https://lms.ksu.edu.sa/ as a Microsoft Word document without using special characters in the name of the file (use only letters, numbers, and underscore).

1- **Coversheet** [2]
   It should show the name of the course, title and number of the experiment, your name and student KSUID number, section number and date of submission.
2- **Objectives** [2]
3- **Circuit Diagrams** [2]
4- **Measurement Methods and Equipment** [4]
   A descriptive **list** of all types of taken measurements, and the equipment used to take them.
   Example: I started out with assembling the circuit shown in Fig x.1. Then I applied a 14-$V_{p\text{-}p}$ sinusoid to the input port of that circuit. The corresponding $V_O(t)$ was obtained using an oscilloscope, and it is shown in Fig x.2.
   Note : Do not copy and paste the procedure!
5- **Measurement Data and Post-Lab Plots** [8]
   It should include Figures, Graphs and Tables**.** Scan your hand-written records of measurements**,** graphs and tables. Do any necessary post-lab plots.
   Note: No need to re-type or re-sketch your results. Your lab-time, hand-written results are enough!
6- **Observations** *(based on your measurements)* [4]
   Example: In step number (…) of procedure (…), I have observed clipping in positive half cycles of $V_O(t)$ when the applied input was a 14-$V_{p\text{-}p}$ sinusoid, but the clipping disappeared when the input's peak to peak amplitude was reduced to 2 V.
7- **Discussion of Observations**
   This is the most important part of your report. Here you should try to interpret/justify your measurements/data and determine whether they are consistent with theory.
   Example: The clipping that I have observed in $V_O(t)$ is due to D_1 operating in the forward region for positive half cycles of $V_i(t)$ and hence maintaining a semi constant drop of 0.7 V value. [4]
8- **Conclusion**
   It should summarize the most important findings you have learned after completing the experiment. It also should include a paragraph about meeting the objectives of the experiment. [4]
9- **References** (if applicable**)**

Please note the following important points:

- Late reports shall not be accepted.
- No reports will be accepted for experiments that you have not actually performed.

Course Learning Outcomes

Upon successful completion of EE 312, the student will hopefully:

CLO 1: Be able to conduct experiments related to the applications, characterization and testing of electronic devices using basic laboratory test equipment.

CLO 2: Understand experimentally obtained characteristic curves, be able to extract circuit models and device parameters from them, and use those models to interpret experimental data.

CLO 3: Understand the role of basic electronic devices in analog and digital applications, and look at some of their possible limitations.

CLO 4: Apply knowledge obtained in the course to design basic electronic circuits, including the design of necessary bias schemes.

CLO 5: Identify the basic analysis types of SPICE, and be able to apply them to explore and verify prototype designs of electronic circuits.

CLO 6: Communicate efficiently by applying technical writing skills to prepare clear, concise, and observation-based lab reports/presentations.

EXPERIMENT

1

Exploring and Testing Junction Diodes

OBJECTIVES:

- To identify the common types of junction diodes.
- To learn how to test junction diodes using a digital multi-meter.
- To explore the basic principle of operation of junction diodes and their use to implement a simple voltage reference.

MATERIALS:

- Laboratory setup, including rastered socket panel
- 2 silicon diodes (e.g., the 1N4001 rectifier diode)
- 1 germanium (Ge) diode
- 1 light emitting diode (LED)
- 1 Zener diode (e.g., 1N4733A)
- 1 resistor (1 kΩ)
- Several wires and bridging plugs

INTRODUCTION

A p-n junction diode is a two-terminal electronic device, which has important applications that we shall explore in this lab. The electrode attached to the p-side of the junction is called the ***anode*** while the one attached to the n-side is called the ***cathode*** (Fig. 1a). The cathode of a diode is usually marked by a band or a dot. It also can be identified based on a simple test using a digital multimeter (DMM).

The diode is characterized by a low resistance to current flow in the forward direction (into the anode and out of the cathode), and very high resistance in the reverse direction. An important feature of a diode biased to conduct a forward current is its ability to maintain its terminal voltage approximately constant over a wide range of currents. Therefore, a forward-biased diode can be approximately modeled by a constant voltage that depends on its type and characteristics. On the other hand, a reverse-biased diode can be modeled by an open circuit.

In this experiment, four types of diodes –the ordinary silicon diode,[1] the germanium diode, the Zener diode and the light emitting diode (LED)– are introduced. A Zener diode is a special type of a silicon diode that is designed and manufactured to operate safely in the reverse breakdown region. An LED is a special type of diode that emits light while conducting a forward current.

One diode or more, depending on the desired dc output voltage, can be used to implement a **voltage reference**. A voltage reference is a circuit that maintains its output dc voltage approximately constant despite reasonable changes in the load current or the input voltage. One could come up with a simple voltage divider to act as voltage reference, but in that case, the output voltage will be very sensitive to even minor changes in the load current or the input voltage.

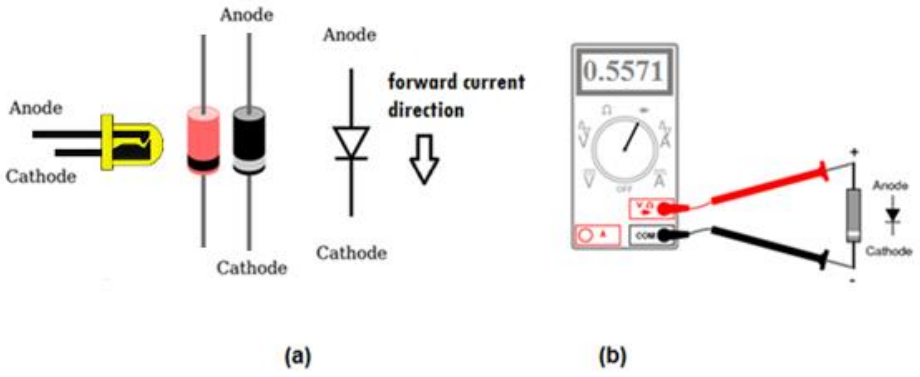


FIGURE 1.1 **(a)** Diode shape and symbol. **(b)** Testing a diode using a DMM.

[1] Diodes for high-power applications, which draw lots of current or rectify high voltages, are called *rectifier diodes*. On the other hand, diodes that are designed to have high switching speeds go by names such as *fast recovery* or *switching diodes* [9].

PROCEDURE A

1. Set your digital multimeter (DMM) to the diode-test mode.
2. Observe and record the open-circuit reading of the DMM in Table 1.1.
3. Connect any type of diode between the red input jack (usually labeled V. Ω.) and the black input jack (labeled COM) of the DMM (Fig. 1.1b).

   If upon connecting a diode to the DMM the reading stays the same as that of an open circuit case (OL in most DMMs), the diode is ideally reverse biased and its cathode terminal should be the one connected to the red jack of the DMM. If the DMM displays a numerical reading (usually less than 3.5 volts) the diode is ideally forward biased, and that reading is the forward voltage drop of the diode–the diode's cathode terminal in this case should be the one connected to the black jack of the DMM.[2]

4. Determine the type of diode based on the approximate expected value of the forward voltage drop of each type, given in Table 1.1b. Record your measurements in that table.

PROCEDURE B

1. Connect the circuit shown in Fig. 1.2, initially using a silicon diode–but without R_L.
2. Make sure that your DMM is on the **dc voltage** measurement mode.
3. Provide your circuit with V_{DD} = 10.0 V using a dc power supply.
4. Use the DMM to verify that the output of the dc power supply is 10.0 V.
5. Use your DMM to measure V_{AB} and $V_{1k\Omega}$ and record their values in Table 1.2.
6. Reverse the diode connection then repeat the previous step.
   - *What is your observation on the necessary condition for a diode to conduct a current?*

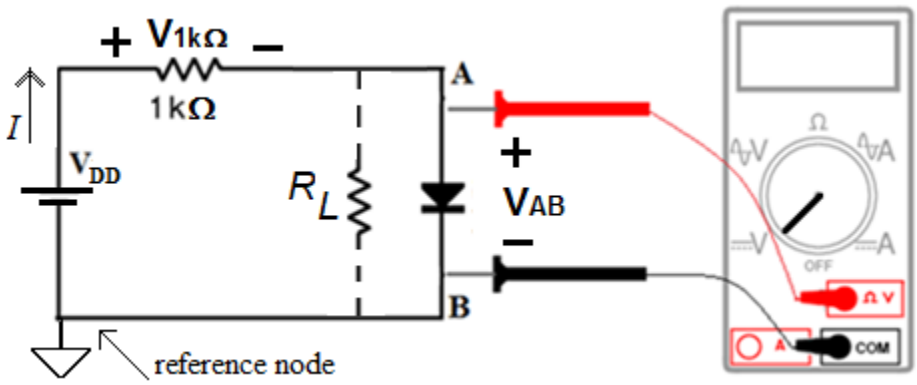


FIGURE 1.2 Exploring the essence of the diode operation.

[2] If while testing a diode the DMM displays similar readings for both directions, this implies that the diode is most probably defective.

7. Connect two ordinary silicon diodes in series back-to-back (i.e., their anodes or connected together) between A and B then measure and record V_{AB} and $V_{1k\Omega}$.

    - *What is your observation on the ability of the back-to-back connection to conduct current?*

8. Connect two ordinary silicon diodes in series, both in the forward direction, between A and B then measure and record V_{AB} and $V_{1k\Omega}$.
9. Use a 10 kΩ resistor R_L to act as a load, connecting it in parallel with the series combination of the two forward biased diodes. Measure and record V_{AB} and $V_{1k\Omega}$.
10. Disconnect the 10 kΩ resistor then connect a 1 kΩ resistor in its place. Measure and record V_{AB} and $V_{1k\Omega}$.

    - *What is you observation on how V_{AB} changes when R_L is changed from ∞ to 10 kΩ, then to 1 kΩ (steps 8, 9 10)?*
    - *What can you say about the behavior of the diode in this circuit?*

RESULTS

TABLE 1.1 Prcodeure A Testing a Diode

DMM Test-Position Reading in Case of an Open Circuit:		
DMM Test-Position Reading in Case of a Reverse-Biased Diode:		
Type of diode	Expected Forward Voltage	Measured Forward Voltage (**Round off** to 3 Decimal Places)
Si	0.55 ~ 0.75 V	
Ge	0.2 ~ 0.4 V	
Zener	0.55 ~ 0.75V	
LED	1.5 ~ 3.5 V	

TABLE 1.2 Prcodeure B Measured Data (Rounded off to 3 Decimal Places)

Step	Type of Diode	Connection Condition	V_{AB} (V)	$V_{1k\Omega}$ (V)	$I = \frac{V_{1k\Omega}}{1\,k}$ (mA)
5	silicon	forward			
6	silicon	Reverse			
7	2 silicon diodes in series	back to back ←→			
Using diodes to implement a voltage reference					
8	2 silicon diodes in series	Forward, without R_L ($R_L = \infty$)			
9	2 silicon diodes in series	Forward, R_L = 10 kΩ			
10	2 silicon diodes in series	Forward, R_L = 1 kΩ			

ASSIGNMENT 1

[CLO 3, CLO 4, CLO 5]

Suppose you need to design a circuit that yields a 3.5 V dc output voltage V_O starting with a dc input V_{IN} of 9 V (See Fig. 1.3). Under no-load condition, the power supplied by the 9 V source should not exceed 100 mW.

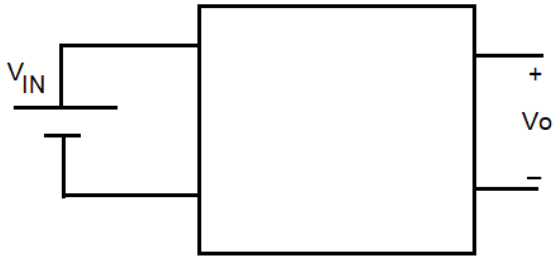


FIGURE 1.3

Design a circuit that uses a standard current-limiting resistor in series with an appropriate number of silicon diodes. Suppose that each of the available silicon diodes to you has the following points on its characteristic curve: (V_1 = 0.585 V at I_1 = 1 mA, V_2 = 0.627 V at I_2 = 2.5 mA, V_3 = 0.65 V at I_3 = 4 mA, V_4 = 0.700 V at I_4 = 11.2 mA).

i. Draw a circuit diagram for your design showing: input, output and the value of a standard resistor.[3]
ii. Find out the color code for the resistor.
iii. Comment on the advantage of using this design compared to using a voltage divider (no diodes).
iv. Simulate your designed circuit using LTspice software.[4]
You can download LTspice from here:
https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html#
You can find an introductory video tutorial here:
https://lms.ksu.edu.sa/bbcswebdav/users/talmadhi/EE312/LTSpice_HW1.mp4
In your simulation, change the default diode to 1N4148. You need to include the circuit's schematic and the simulation results of your design in your assignment submission. To do that in LTspice, click on Tools >> Copy bitmap to Clipboard. Then paste the copied image in your Word document.

[3] See Appendix F.
[4] See the introduction of experiment 5 for further information on LTspice.

EXPERIMENT

2

Terminal Characteristics Of Junction Diodes

OBJECTIVES:

- To experimentally obtain the *i-v* characteristic curves for a general-purpose junction diode and a Zener diode.
- To get acquainted with Zener diodes and learn how they differ from ordinary diodes.
- To be able to extract a piecewise-linear model from an *i-v* characteristic curve.

MATERIALS:

- Laboratory setup, including rastered socket panel
- 1 ordinary silicon diode (e.g., the 1N4001 rectifier diode)
- 1 Zener diode (e.g., 1N4733A)
- 1 resistor (1 kΩ)
- Several wires and bridging plugs

INTRODUCTION

Figure 2.1 shows the $i - v$ relationship of a silicon diode. This relationship consists of three distinct *regions of operation*: The forward-bias region ($v > 0$), the reverse-bias region ($v < 0$), and the breakdown region ($v < -V_{ZK}$). In the forward region the $i - v$ relationship is closely approximated by

$$i = I_S\left(e^{\frac{v}{nV_T}} - 1\right) \qquad (2.1)$$

where I_S is the saturation current, V_T is the thermal voltage ≅ 26 mV at T = 300 K, n is the emission coefficient whose value $1 \le n \le 2$. The diode forward characteristic can be approximated by an equivalent circuit based on a piecewise-linear model which consists of a **battery** V_{D0} **plus a resistance** r_D.(Fig. 2.2a). The model parameters V_{D0} and r_D can readily be calculated if we know two **operating points (Q-points)** on the forward characteristic curve. The parameters are not unique for a given diode because they depend on the current range over which they are calculated.

The breakdown region is characterized by a near-vertical line (voltage-source behavior), which is desirable if the diode is to be used in voltage regulation. Diodes specifically manufactured to operate in this region are commonly called **Zener diodes**. Commercial Zener diodes are available having **nominal** Zener voltages of 2.4 to 200 V.

A Zener diode operating in the breakdown region can be modeled by an **equivalent circuit** based on a piecewise-linear approximation (Fig. 2.2b). The inverse of the slope of the breakdown region characteristic determines the Zener **dynamic resistance** r_Z. Smaller r_Z means steeper characteristic and consequently smaller $\Delta V_Z = \Delta I_Z \times r_Z$, which suggests that we can use a Zener diode in that region as a **voltage reference** or as a **voltage regulator**.

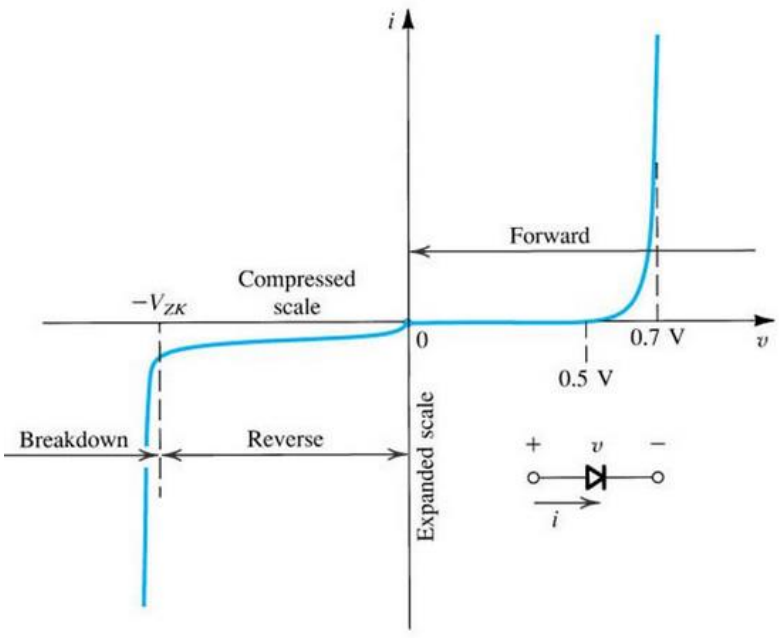
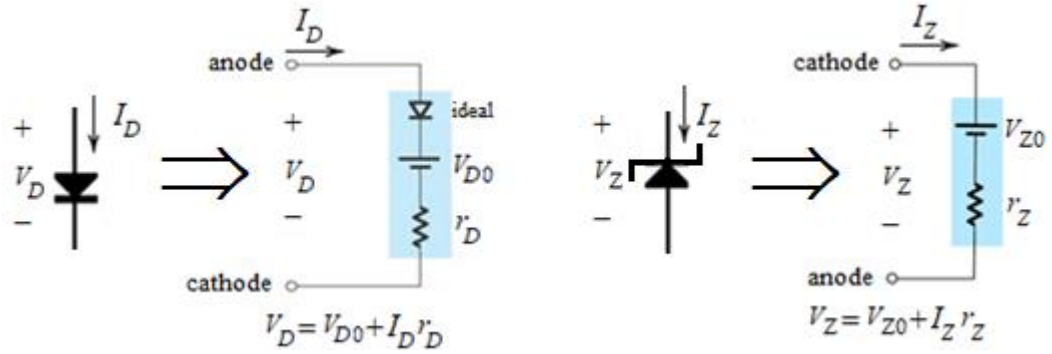


Figure 2.1 The diode i-v characteristic curve [1].

PROCEDURE

1. Using a digital multimeter (DMM), measure and record the actual value of *R*.
2. Connect the circuit shown in Fig. 2.3 initially with an ordinary silicon diode.
3. Using a dc power supply, start out by applying a V_{DD} of 15 V to your circuit.
4. Using a digital multimeter, measure and record V_D and V_R in Table 2.1.
5. Calculate the corresponding value of I_D using Ohm's law. **Round off** the measured values of voltages and calculated values of current to **3 decimal places**.
6. For the same value of V_{DD}, replace the ordinary silicon diode with a Zener diode and record V_{DZ} and V_R in Table 2.2.
7. Adjust the dc power supply to obtain a V_{DD} of 7 V.
8. Using a digital multimeter, measure and record V_{DZ} and V_R in Table 2.2.
9. For the same value of V_{DD}, replace the Zener diode with the ordinary silicon diode and record V_D and V_R in Table 2.1.
10. Do the necessary steps to fill in all entries of Table 2.1 and Table 2.2.
    Note: For the negative values of V_{DD} you will need to swap the dc supply leads on the board. However, the reference polarities for V_R and V_D remain unchanged.
11. Plot I_D vs. V_D for both diodes using MATLAB (see Appendix B). Label the three regions of operation on the graph.



(a) (b)

Figure 2.2 Linear model of **(a)** a forward–biased diode, **(b)** a Zener in breakdown.

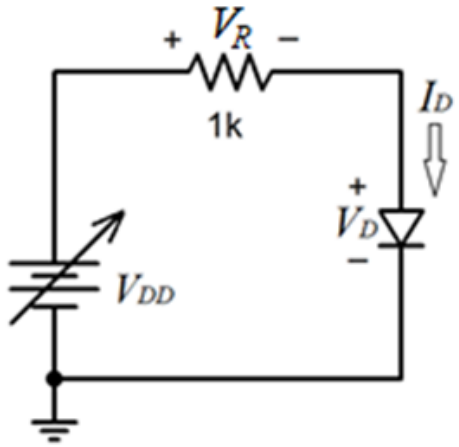


Figure 2.3 Circuit for measuring the i-v characteristics.

RESULTS

Table 2.1 Ordinary Silicon Diode *i-v* Measured Data **(Rounded Off to 3 Decimal Places)**

V_{DD} (V)	V_D (V)	V_R (V)	$I_D = V_R/R$ (mA)	V_{DD} (V)	V_D (V)	V_R (V)	$I_D = V_R/R$ (mA)
15				-2			
7				-3			
1.6				-3.5			
0.7				-4			
0.5				-4.5			
0.2				-7			
0	0	0	0	-15			

Table 2.2 Zener Diode *i-v* Measured Data **(Rounded Off to 3 Decimal Places)**

V_{DD} (V)	V_D (V)	V_R (V)	$I_D = V_R/R$ (mA)	V_{DD} (V)	V_{DZ} (V)	V_R (V)	$I_{DZ} = V_R/R$ (mA)
15				-2			
7				-3			
1.6				-3.5			
0.7				-4			
0.5				-4.5			
0.2				-7			
0	0	0	0	-15			

ASSIGNMENT 2

[CLO 3, CLO 4]

1. Use two pairs of $i - v$ measurements ($V_D > 0.5$) in the forward region (Table 2.1)[5] to calculate *n* for the silicon diode, which can be found using the following equation:

$$n = \frac{V_{D2} - V_{D1}}{2.3 \times V_T \times \log\left(\frac{I_{D2}}{I_{D1}}\right)} \qquad (2.2)$$

2. Use one pair of measurement and *n* to calculate I_S for the silicon diode using Eq. (2.3).

$$I_S = I_D \times e^{\frac{-V_D}{nV_T}} \qquad (2.3)$$

3. Extract a piecewise-linear model for the silicon diode in the forward region (Fig. 2.2a) using (V_{D1}, I_{D1}) that you have measured at V_{DD} = 1.6 V and (V_{D2}, I_{D2}) that you have measured at V_{DD} = 15 V. This can easily be done as follows:

   i. Calculate r_D given that $r_D = \frac{1}{Slope} = \frac{\Delta V_D}{\Delta I_D} = \frac{V_{D2} - V_{D1}}{I_{D2} - I_{D1}}$

   ii. Calculate V_{D0} using either

   $V_{D1} = V_{D0} + I_{D1} \times r_D$ or $V_{D2} = V_{D0} + I_{D2} \times r_D$

4. For V_{DD} = 7 V, use the model you have obtained for the diode to calculate I_D and V_D.
5. Calculate the error % in the V_D and I_D obtained in (4) with respect to the measured values that you have recorded in Table 2.1 Tabulate your results as shown below.

Method	V_D (V)	I_D (mA)	V_D error %	I_D error %
Measured (from Table 2.1)			0	0
Using the piecewise-linear model approximation				

6. Extract a piecewise-linear model for the Zener diode **in the reverse breakdown region** (Fig.2.2b). Use the absolute values of the currents and voltages that you have measured at V_{DD} = -7 V and V_{DD} = -15 V. This can easily be done as follows:

   i. Calculate r_Z given that $r_Z = \frac{1}{Slope} = \frac{\Delta|V_{DZ}|}{\Delta|I_{DZ}|}$ (in reverse breakdown)

   ii. Calculate V_{Z0} using either

   $|V_{DZ1}| = V_{Z0} + |I_{DZ1}| \times r_Z$ or $|V_{DZ2}| = V_{Z0} + |I_{DZ2}| \times r_Z$

[5] Please attach a copy of that table in your submittal for this assignment.

EXPERIMENT

3

Limiting Circuits

OBJECTIVES:

- To explore the basic principles of some limiting (clipping) circuits and be able to predict their responses.
- To experimentally obtain and examine the output waveforms and the voltage transfer characteristics of some typical circuits of that type.
- To be able to design and implement a circuit to satisfy a given limiting transfer characteristic.

MATERIALS:

- Laboratory setup, including rastered socket panel
- 2 silicon diodes (e.g., the 1N4001 rectifier diode)
- 2 Zener diode (e.g., 1N4733A)
- 1 resistor (1 kΩ)
- Several wires and bridging plugs

INTRODUCTION

Limiting or clipping is a function performed by a circuit that has the ability to limit or clip off portions of a signal that are above or below a specified level [5]. A junction diode is a suitable candidate for this type of circuits because, as we have learned, once it conducts enough current it tends to have little variations in its voltage, voltage reference behavior.

Fig. 3.1 shows the general voltage transfer characteristic (VTC) for a **double limiter**. The circuit acts linearly for inputs larger than the **lower threshold** and less than the **upper threshold**, $(V_O^-/A_V) < v_I < (V_O^+/A_V)$. If, however, $|v_I|$ exceeds the magnitude of the threshold levels, the output voltage is limited or clamped to the **limiting levels**. If there is no load connected across its output port, a limiter will have a unity slope A_V in the linear region of its VTC, and consequently the threshold levels will be equal to the limiting levels.

The limiting levels of a given limiting circuit can designed to meet a given specification. Toward that end, the diode forward drop (0.6–0.8 V for a silicon diode) and/or the nominal Zener voltage V_Z (a list of which is given in Appendix E) can be utilized to obtain specified limiting levels of a desired transfer characteristic.

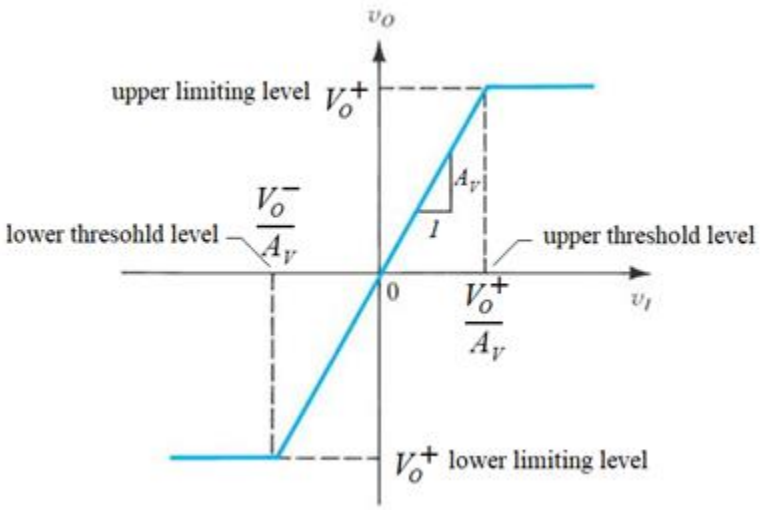
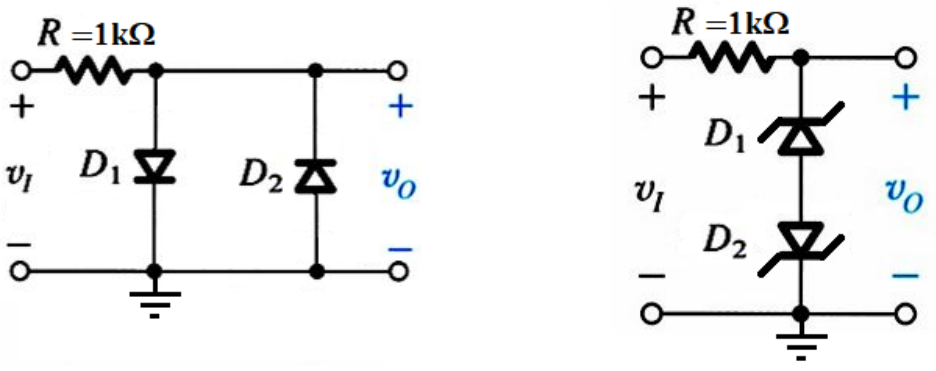


Figure 3.1 General transfer characteristic for a double limiter circuit.



(a) (b)

Figure 3.2 **(a)** Antiparallel-diode double limiter. **(b)** Double-anode Zener limiter.

PROCEDURE A

1. Assemble the circuit shown in Fig. 3.2a.
2. Turn on your oscilloscope.
3. Use a coaxial cable to connect the circuit's input to channel 1 (CH 1) of the scope.
4. Use another cable to connect the circuit's output to channel 2 (CH 2) of the scope. *The black ground leads of the two coaxial cables should be connected to the circuit's reference node, i.e. to the circuit's ground.*
5. Set CH 1 coupling selector to GND, and then use the POSITION 1 control (knob) to align the base line (zero-reference trace) at the midpoint of the screen.
6. Set CH 2 coupling selector to GND, and then use the POSITION 2 control to align the zero-reference trace at the midpoint of the screen.
7. Set the coupling selectors of both channels to DC (make sure that the GND and AC coupling indicator lights are off).
8. Use the vertical sensitivity (VOLTS/DIV) controls of CH 1 and CH 2 to set their sensitivities at **0.5 V/DIV (500 mV/DIV)**.
9. Use the time base (TIME/DIV) control to set the timebase speed at **1 ms/DIV**.
10. Select the buttons AC and CH 1 in the TRIGGER select area (TRIG. MODE).
11. Display both channel simultaneously by setting your scope to the **DUAL mode**.
12. Use a coaxial cable to connect the output of a function generator to the input of your circuit, and then turn it on. *The black ground lead of the coax cable should be connected to the circuit's reference node, i.e. to the circuit's ground.*[6]
13. Set the input signal type to sinusoidal. Then, set the input frequency at 200 Hz and its amplitude at 0.6 $V_{p\text{-}p}$ (peak to peak).
14. Is there any difference between the waveforms of $v_I(t)$ and $v_O(t)$? Why?

15. Gradually increase the amplitude of the input until you reach 3 $V_{p\text{-}p}$.
16. Record $v_I(t)$ and $v_O(t)$ waveforms on Fig. 3.3a.
17. Closely examine the shape of $v_O(t)$. Take note of how many major divisions M_D and minor divisions m_d the positive peak value is displaced from the zero-reference level (at the screen's midpoint). Calculate the circuit's **upper limiting levels** as follows:

$M_D =$

$m_d =$

$\text{Displacement} = M_D + m_d \times 0.2 =$

$\text{Upper Limiting Level } (V_O^+) = \text{Displacement} \times \text{Sensitivity}$

$=$

[6] Be careful! Putting a circuit element (e.g. resistor, diode, etc.) between the ground leads of cables connected to lab equipment will short circuit that element and is considered hazardous!

18. Take note of how many major divisions M_D and minor divisions m_d the negative peak value is displaced from the zero-reference level. Calculate the circuit's **lower limiting levels** as follows:

M_D =

m_d =

Displacement = - (M_D + m_d × 0.2) =

Lower Limiting Level (V_O^-) = Displacement × Sensitivity

=

19. Set the scope to **XY mode**, and then set the coupling of both channels to GND. Use the X-POSITION control to align the dot-shaped beam with the origin. Set the coupling controls of both channels back to DC.
20. Record the displayed voltage transfer characteristic (VTC) on Fig. 3.3b.
21. Set your scope back to DUAL mode.
22. Write down what you observe when D_2 is disconnected.

PROCEDURE B

1. Turn off your function generator.
2. Modify your circuit to implement the circuit diagram shown in Fig. 3.2b.
3. Set the vertical sensitivities of the two channels of the scope to **2 V/DIV.**[7]
4. Turn on the function generator. Is there any difference between the waveforms of v_I(t) and v_O(t)? Why?

5. Gradually increase the amplitude of the input until you reach 15 $V_{p\text{-}p}$.
6. Record v_I(t) and v_O(t) waveforms on Fig. 3.4a.
7. Examine the shape of v_O(t), then find out the circuit's **upper** and **lower limiting levels**.

Upper Limiting Level (V_O^+) = Displacement × Sensitivity

=

Lower Limiting Level (V_O^-) = Displacement × Sensitivity

=

8. Put your scope on XY mode to display the VTC of your circuit.
9. Record the displayed VTC on Fig. 3.4b.
10. Theoretically, what is the expected value of V_O^+ in terms of V_Z? Calculate V_Z using the measured value of V_O^+ in step 7 of procedure B.

[7] Increasing the volts/division leads to decreasing the sensitivity, which enables us to see signals of larger amplitudes.

RESULTS

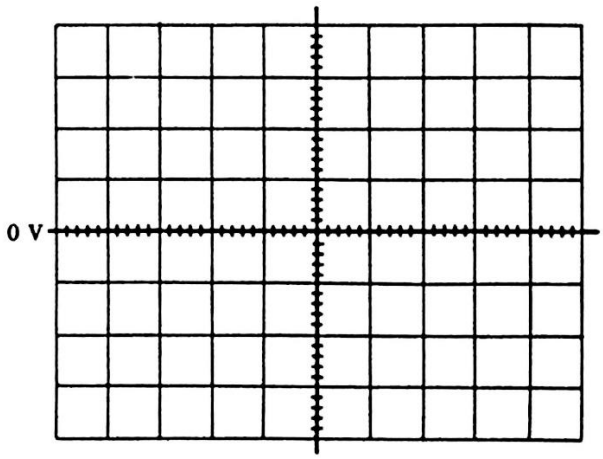


Figure 3.3a

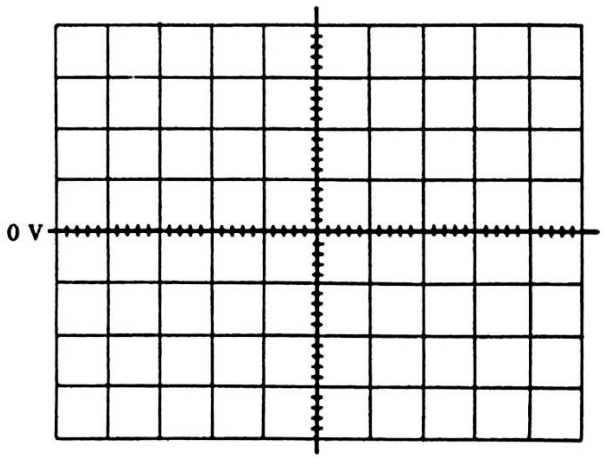


Figure 3.3b

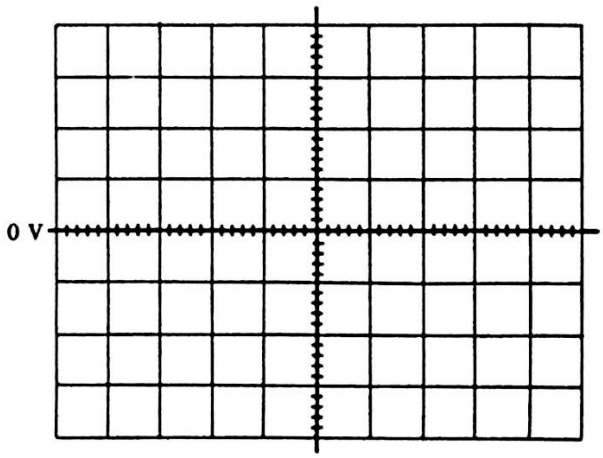


Figure 3.4a

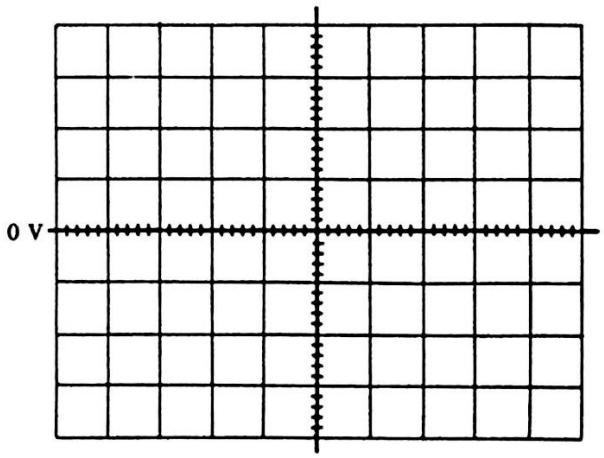


Figure 3.4b

ASSIGNMENT 3

[CLO3, CLO 4, CLO 5]

1. Design and sketch a limiting circuit whose output is kept within the limits of the following range: $-2.1\ \text{V} \pm 5\% \leq V_O \leq 5.4 \pm 5\%\ \text{V}$,
   i. using only a resistor and appropriate number of regular silicon diodes, then
   ii. using only a resistor, an appropriate number of regular silicon diodes and a Zener diode operating in the reverse breakdown region.

- Assume a forward voltage drop of 0.7 V for both types of diodes and $V_Z = 4.7$ V for the Zener diode operating in reverse breakdown.

- *Hint:* Use two branches of appropriately connected diodes, branch A that conducts current only for positive half cycles of the input to give you the upper limiting level and branch B that conducts current only for negative half cycles of the input to give you the lower limiting level.

7. Perform an LTspice *transient* as well as *DC sweep* analyses to verify that your proposed circuits meets specifications. In your simulation, use diode IN4148 for a regular silicon diode and 1N750 for a Zener diode:
   - To apply a sinusoidal waveform, right click on the voltage source >> click on advanced, and then select SINE. Fill in the required parameters as follows: (DC offset = 0, Amplitude = 10, Freq = 100, Tdelay = 0, Theta = 0, Phi = 0, Ncycles = 3).
   - To obtain the transient analysis, Go to Edit >> SPICE analysis, make sure that the Transient tab is selected, and then fill in the required fields, which are: (Stop time = 30m , Time to start saving data = 0, Maximum Timestep = 0.3m).
   - Run the simulation. Click on Tools >> Copy bitmap to Clipboard. Then paste the copied image in your Word document. Do that for the schematic window as well as the waveform window.
   - To obtain the DC sweep, Go to Edit >> SPICE analysis, make sure that the DC sweep tab is selected, use a start value of -10, a stop value of 10 and an increment of 20m.[8]
   - Run the simulation. Click on Tools >> Copy bitmap to Clipboard. Then paste the copied image in your Word document. Do that only for the waveform window.
   - From the above simulation results, find the upper and lower limiting levels.

   Watch the following video if you need further help:
   https://lms.ksu.edu.sa/bbcswebdav/users/talmadhi/EE312/LTSPice_HW3.mp4

[8] See the introduction of experiment 5 for further information on LTspice.

EXPERIMENT

4

Rectifiers

OBJECTIVES:

- To experimentally explore an important application of diodes, namely the rectifier
- To understand the importance of filtering and voltage regulation in the process of ac to dc conversion.
- To learn and apply some practical design tips for designing full-wave rectifier circuits.

MATERIALS:

- Laboratory setup, including rastered socket panel
- 1 center-tapped transformer
- 2 silicon diodes (Si) (e.g., the 1N4001 rectifier diode)
- 2 electrolytic capacitors (10 μF, 470 μF)
- 2 resistors (4.7 kΩ, 270 Ω)
- Several wires and bridging plugs

INTRODUCTION

Electronic equipment needs dc power supply to operate. A block diagram of such a system is shown in Fig. 4.1 [1]. This system involves rectification, filtering and voltage regulation.

A **power transformer** is used to step down the input ac voltage and provide electrical isolation, which is important for safety. A **diode rectifier** uses the unidirectional-current property of diodes to convert an input sinusoid to a unipolar but pulsating output. Acting as a simple low-pass filter, a **filter capacitor** is used to reduce the **ripple** (pulsation) of the resulting output waveform.

The peak-to-peak output voltage ripple V_r is inversely proportional to R_L–directly proportional to the dc load current I_L, and inversely proportional to the capacitance C of the filter capacitor. Therefore, a **voltage regulator** is needed to help keep the dc output voltage fixed despite possible variations in the load current and/or the ac input voltage. We shall examine the effect and benefits of voltage regulation in experiment 5.

There are two main implementations of a full-wave rectifier: the one that utilizes a **center-tapped** transformer and requires only two diodes (see Fig. 4.2b) and the **bridge rectifier** that does not require a center-tapped transformer but requires four diodes. We shall explore the bridge rectifier in experiment 5.

Two important parameters are needed to be specified when an engineer needs to select diodes for a given rectifier design: the **p**eak **i**nverse **v**oltage (**PIV**) and current-handling capability. The PIV is the maximum reverse voltage that the diode ever experiences in a given circuit [4].

A manufacturer's **data sheet** gives detailed information on a device so that it can be used properly in a given application. Appendix C shows the datasheet for general-purpose rectifier diodes (1N4001 – 1N4007). $\mathbf{V_{RRM}}$ is the maximum peak repetitive reverse voltage that can be applied across the diode. $\mathbf{I_{F(avg)}}$ is the maximum average rectified forward current at T_A=75°C. $\mathbf{I_{FSM}}$ is the maximum not repetitive forward **surge** current the diode can sustain. A surge resistor R_{surge} is usually used to limit the maximum possible initial charging current of the capacitor, which occurs when v_S(t) is at its peak V_S, well below $\mathbf{I_{FSM}}$.

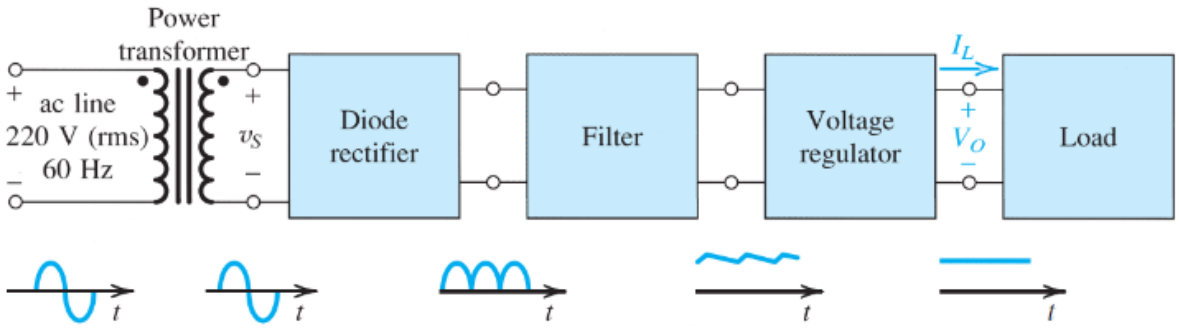


Figure 4.1 A block diagram of a dc power supply [1].

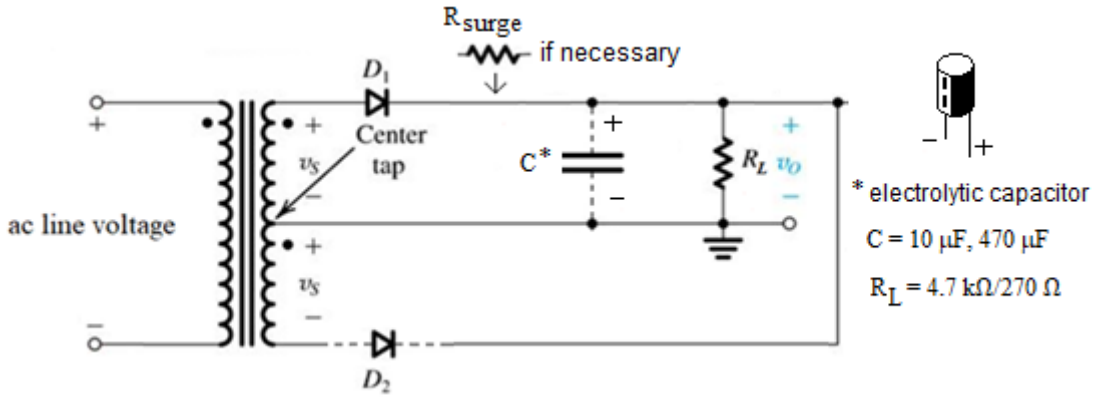


Figure 4.2 Rectifier circuit which uses a center-tapped transformer.

PROCEDURE

The Half-Wave Rectifier:

1. Assemble the circuit shown in Fig. 4.2, with R_L = 4.7 kΩ, and initially without connecting D_2 and C. **Do not connect the transformer to ac power until the instructor checks your circuit out.**
2. Turn on your scope, and set both channels to *setting 1* (Table 4.1).
3. Use a coaxial cable to display v_S(t) on CH 1 of the scope, and another cable to to display v_O(t) on CH 2.
4. Connect the transformer to ac power .
5. Put the scope on DUAL mode, then record v_S(t) and v_O(t) waveforms on Fig. 4.3.
6. Put the scope on X-Y mode, then record the voltage transfer characteristic on Fig. 4.4.

The Full-Wave Rectifier:

7. Connect D_2, put the scope on DUAL mode, and record v_S(t) and v_O(t) on Fig. 4.5.
8. What is the frequency of the v_O(t) waveform?
9. Put the scope on X-Y mode, and record the voltage transfer characteristic on Fig. 4.6.

The Effect of Filtering:

10. Put the scope on DUAL mode, then connect a 10 μF electrolytic capacitor in parallel with R_L; the capacitor lead marked with a negative sign should be connected to ground. Record v_S(t) and v_O(t) waveforms on Fig. 4.7.
11. Replace the 10-μF capacitor with a 470-μF one, then record v_S(t) and v_O(t) waveforms on Fig. 4.8.

The Effect of Reducing R_L:

12. Set channel 2 of your scope to *setting 2* (Table 4.1). Replace the 4.7 kΩ resistor with a 270 Ω one. Observe and comment on how the ripple changes if R_L is reduced.

TABLE 4.1 Oscilloscope settings

Setting	Sensitivity (VOLT/DIV)	Timebase Speed (ms/DIV)	Coupling	Zero Reference Position	Trigger
1	5	5	dc	center	Line (AC)
2	2	5	dc	bottom	Line (AC)

RESULTS

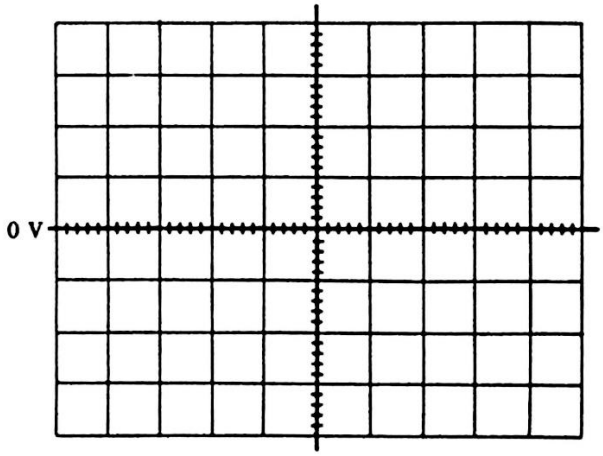


Figure 4.3

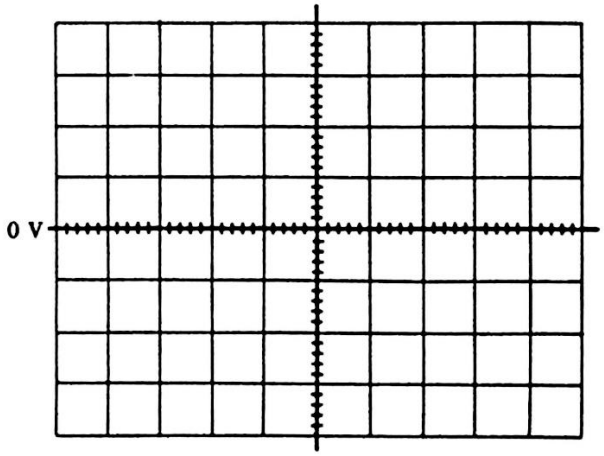


Figure 4.4

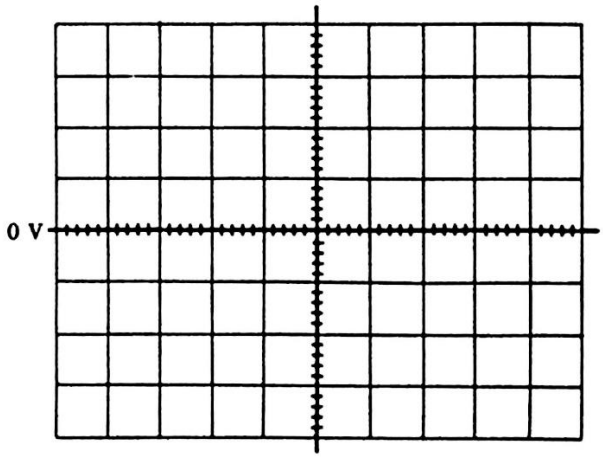


Figure 4.5

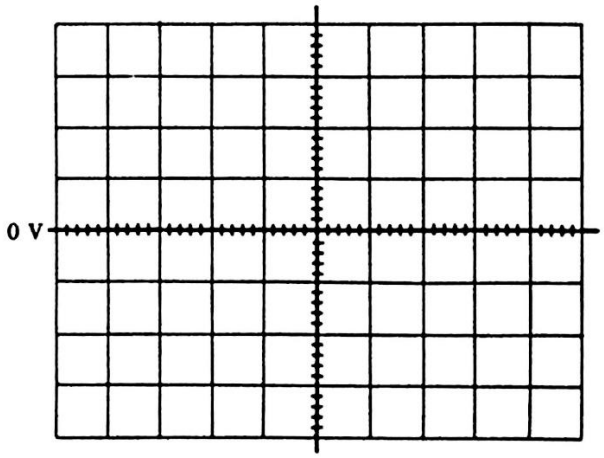


Figure 4.6

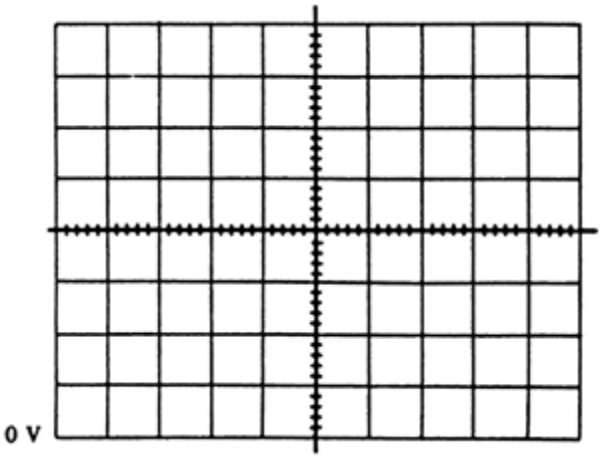


Figure 4.7

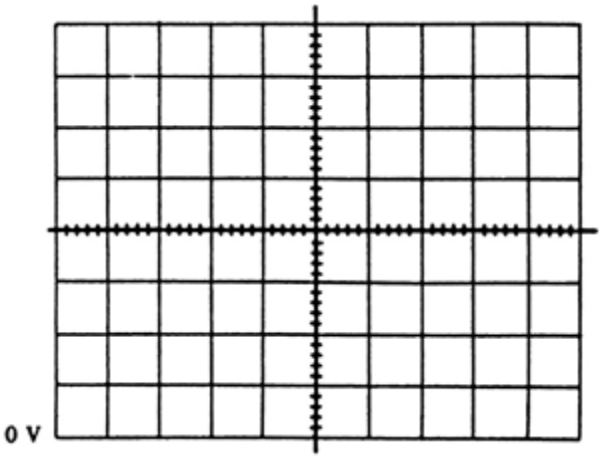


Figure 4.8

DESIGN TIPS

Use the following checklist to complete a rectifier design−either full wave (FW) or half wave (HW)−given the frequency *f*, the value of the load resistance R_L, the secondary ***peak*** voltage V_s of the transformer and the output voltage ripple ***peak-to-peak*** V_r .

1. If not given, determine the dc component of the load current I_L using the following equation:

$$I_L \cong \frac{V_s}{R_L} \qquad (4.1)$$

2. Determine *C* using the following equation:

$$C = \frac{1}{f} \times \frac{I_L}{V_r} = \frac{1}{60} \times \frac{I_L}{V_r} \qquad \text{(HW)} \qquad (4.2a)$$

$$C = \frac{1}{2f} \times \frac{I_L}{V_r} = \frac{1}{120} \times \frac{I_L}{V_r} \qquad \text{(FW)} \qquad (4.2b)$$

3. Select a standard value of *C* from the table given in Appendix F.
4. Determine the diode average forward current using the following equation:

$$i_{Dav} \cong I_L \left(1 + \pi \sqrt{\frac{2V_s}{V_r}} \right) \qquad \text{(HW)} \qquad (4.3a)$$

$$i_{Dav} \cong I_L \left(1 + \pi \sqrt{\frac{V_s}{2V_r}} \right) \qquad \text{(FW)} \qquad (4.3b)$$

5. Determine the PIV for the diode, which depends on which rectifier circuit you plan to build. Search your textbook [1] for more information.[9]
6. Determine the $\mathbf{V_{RRM}}$ rating of the diode based on the PIV. A good practice is to have $\mathbf{V_{RRM}}$ = 1.5 PIV
7. Determine $\mathbf{I_{F(avg)}}$ of the diode. A good practice is to have $\mathbf{I_{F(avg)}}$ = 1.5 i_{Dav}
8. Use Appendix D to look for a rectifier diode that has at least the same ratings as determined in the above two steps.
9. Calculate the maximum surge current (neglecting the diode resistance) using:

$$I_{surge} = \frac{V_S}{\mathrm{R_{SW}}} \qquad (4.4)$$

   where R_{SW} stands for a single secondary winding resistance.
10. Search the internet for a pdf version of the datasheet of that diode, and then find out the value of $\mathbf{I_{FSM}}$. Make sure that $I_{\text{surge}} < 0.8\ I_{FSM}$; otherwise determine R_{surge} of a standard value needed to limit the diode surge current using:

$$R_{surge} + R_{SW} = \frac{V_S}{0.8 \times \mathrm{I_{FSM}}} \qquad (4.5)$$

---

[9] For the circuit shown in Fig. 4.2, PIV = V_S-0.7-(-V_S) ≅ 2V_S, where V_S represents the peak value of v_S(t). Check for yourself!

ASSIGNMENT 4

[CLO3, CLO 4]

Using the design tips given on the previous page, design a **full-wave** rectifier with a filter capacitor (Fig. 4.2) to supply a dc load of I_L = 100×SN mA, where SN is your serial number in your section, at 9V dc with a ripple of 0.5 $V_{p\text{-}p}$. The input ac voltage available to you has 220 V (rms value), and you have a center-tapped transformer that has a turns ratio[10] between the primary and one of the secondary windings *Np*/*Ns1* = 22; for each of the secondary windings, R_{SW} = 1 **Ω**.

a. What is the peak voltage between one terminal and the center tap of the secondary winding, i.e. V_s?
b. Calculate the capacitance of the required capacitor to keep the peak-peak ripple voltage as given above.
c. Calculate $\mathbf{I_{F(avg)}}$ for the type of diode you are going to use to build the circuit.
d. Calculate $\mathbf{V_{RRM}}$ for the type of diode you are going to use to build the circuit.
e. Look for a rectifier diode that can be used for your design using the table given in Appendix D.
f. Search the net for a pdf version of the selected diode datasheet, and then look up its maximum surge current $\mathbf{I_{FSM}}$.
g. Calculate I_{surge}; do you need a surge resistor R_{surge}? Calculate its value if necessary.
h. What is the expected output dc voltage?
i. If the expected dc output voltage is not equal to 9 V dc, search the net for the "7809 voltage regulator" datasheet, or look at this page:

   https://components101.com/regulators/7809-voltage-regulator-pinout-datasheet-specifications

j. Draw the complete system, i.e. the transformer, the rectifier, the capacitor, and the voltage regulator.

[10] Recall that $V_S / V_P = N_{S1} / N_P$.

EXPERIMENT

5

Computer Simulation of Electronic Circuits

OBJECTIVES:

- To learn how to simulate electronic circuits using freely-available online design tools, the LTspice® software as an example.
- To see why a voltage regulator is needed in ac to dc conversion systems with the aid of simulation as a study tool.

MATERIALS:

- A PC or a laptop with a LTspice® installed

INTRODUCTION

In this experiment, we shall explore the importance of using a **voltage regulator** in the process of ac to dc conversion with the aid of computer simulation. We shall implement a simple voltage regulator using a Zener diode. If operated in the reverse breakdown, a Zener diode effectively behaves like a voltage reference owing to the semi-vertical shape of its characteristic curve in that region, which implies that the Zener diode will maintain a constant voltage, V_Z, across its terminals for a wide range of reverse breakdown currents.

LTspice® is a high performance SPICE simulation software, schematic capture and waveform viewer with enhancements and models for easing the simulation of analog circuits. Included in the download of LTspice are macromodels for a majority of Analog Devices switching regulators, amplifiers, as well as a library of devices for general circuit simulation.[11]

To place a new component on your schematic, you can either press F2 or go to Edit >> Component. To place a new resistor on your schematic, you can either press 'R' on the keyboard or go to Edit >> Resistor. To place a new capacitor on your schematic, you can either press 'C' or go to Edit >> Capacitor. To place a new inductor on your schematic, you can either press 'L' or go to Edit >> Inductor. To place a new diode on your schematic, you can either press 'D' or go to Edit >> Diode. To change the model of the diode, right click on it, and then click on Pick New Diode. To place a new voltage source on your schematic, you can either press 'v' or press F2, and then select voltage, then click OK. To place a ground (GND) on your schematic, you can either press 'G' or go to Edit >> Place GND. To wire the components, you can either press F3 or go to Edit >> Draw wire.

When you wish to move, mirror, rotate, drag or delete objects, first select the move, drag or delete command form the top Toolbar. Then you can select an object by clicking on it. You can select multiple objects by dragging a box about them. The program will stay in the move, drag, or delete mode until the right mouse button is clicked or the Esc key is pressed.

Simulating a circuit by LTspice involves the following basic steps:

1. Opening a new schematic (File >> New Schematic), placing required components, wiring them, and adding a ground.
2. Setting an appropriate SPICE analysis (Edit >> SPICE Analysis). The basic analysis types are: DC operating point (DC op pnt), DC sweep, AC analysis, and transient.
3. Running the simulation, and then selecting the desired response.
4. Saving the circuit before closing the program.

[11] https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html#

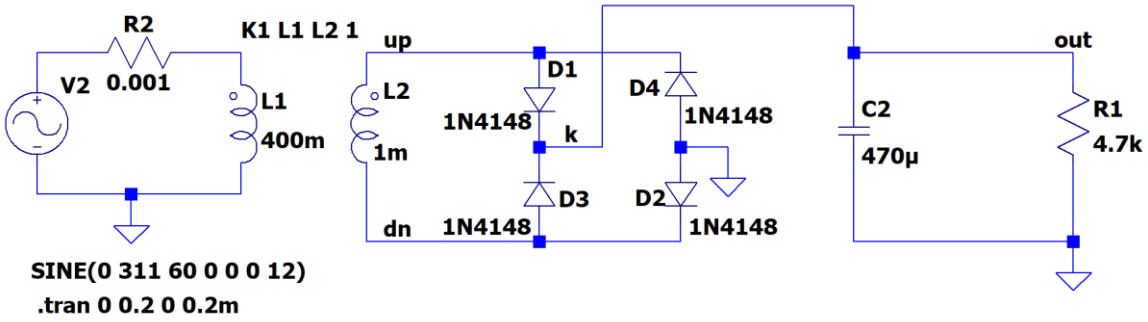


Figure 5.1 Bridge rectifier circuit.

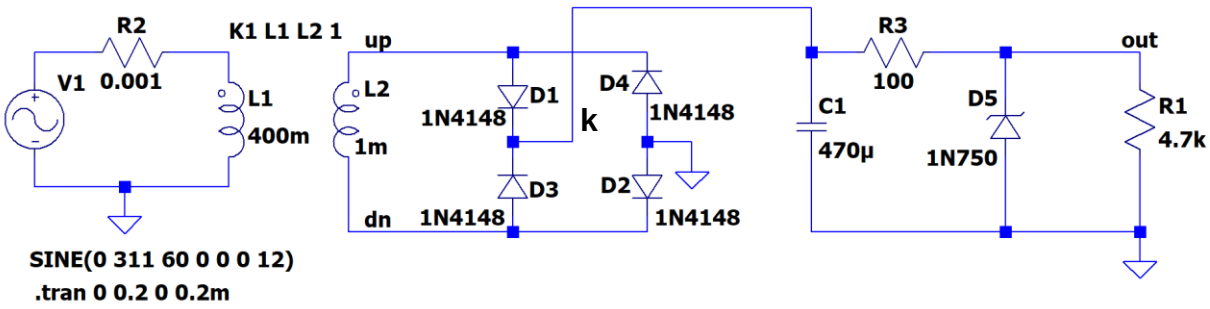


Figure 5.2 Regulated power supply.

PROCEDURE

1. Double click the LTspice icon on the desktop.
2. Go to File >> New Schematic.
3. First, you have to add all components required to build the circuit (Fig. 5.1) on your schematic, except for the capacitor.[12] Note: to add the coupling coefficient between the two inductors, go to Edit >> SPICE directive, and type: K1 L1 L2 1.
4. Wire all components, add ground (GND), and label the **up**, **dn**, and the **out** nodes.
5. To adjust a component value, right click on it then type the required value. In SPICE, meg stands for 1e6 (mega), k stands for 1e3 (kilo), m stands for 1e-3 (milli), u stands for 1e-6 (micro), n stands for 1e-9 (nano), and p stands for 1e-12 (pico).
6. To adjust the voltage source parameters, right click on it, and then fill in the required fields, which are: (DC offset = 0, Amplitude = 311, Freq = 60, Tdelay = 0, Theta = 0, Phi = 0, Ncycles = 12).
7. Go to Edit >> SPICE analysis, and then fill in the required fields, which are: (Stop time = 0.2 , Time to start saving data = 0, Maximum Timestep = 0.2m).
8. To run your simulation, go to Simulate >> run.

[12] See the introduction on the previous page, or watch:
https://lms.ksu.edu.sa/bbcswebdav/users/talmadhi/EE312/LTSpice_HW1.mp4

9. To see the waveform of the output voltage, click on the **out** node on the circuit schematic.
10. To see the input (at the secondary winding of the transformer, V(up) - V(dn)), right click on the waveforms window, then select Add Traces, then select **V(up)**, then put the mouse pointer in the *Expression(s) to add* field and type '-', then select **V(dn)**, then click OK.
11. To see the voltage waveform across one of the diodes (D1 for example), right click on the waveforms window, then select Add Traces, then select **V(up)**, then put the mouse pointer in the *Expression(s) to add* field and type '-', then select **V(out)**, then click OK. What is the peak inverse voltage **PIV** for D1? Note that it is equal in magnitude to the peak amplitude across the transformer secondary winding. The **PIV** must be less than the **VRRM** of the diode by at least 25% (See Fig. 5.3 for the absolute maximum ratings for the N4148).
12. Connect the capacitor as shown in Fig 5.1, and rerun the simulation to see how that affects the ripple in the output voltage waveform. Experiment with lower values of capacitance (10 μF for example) to see the effect on the output waveform ripple.
13. Put the mouse pointer on diode D1 (note how its shape changes to a clamp meter) then click on the diode. The resulting waveform is the diode's current. Note how the current takes a surge value at the beginning of the simulation.[13] The diode must have an $\mathbf{I_{FSM}}$ rating less than that surge current (See Fig. 5.3 for the absolute maximum ratings for the N4148). If, however, the surge current is larger than $\mathbf{I_{FSM}}$ of the diode, a properly sized surge resistance must be used between the node labeled **out** and node **k**.
14. On the waveform window, click and drag your mouse diagonally to show only the waveform for time greater than 100 ms. Put the mouse pointer on I(D1), press Ctrl then click on I(D1). You should see a small window displaying the average value of the current waveform. That average current should be less $\mathbf{I_{F(AV)}}$ rating of the diode by at least 25%.
15. Press Ctrl+E to return to the original view.
16. Delete the I(D1) trace and the V(up)-V(out) trace.
17. Decease the value of R_1 to 270 Ω and rerun to see how that affects the ripple in the output.
18. Add a voltage regulator to your dc supply circuit as shown in Fig. 5.2. Change R_1 back to 4.7 kΩ. Rerun the simulation.

- *What does the output waveform look like? How is the output voltage level related to V_Z of the Zener diode?*

19. Reduce R_1 to 270 Ω and rerun to see how that affects the ripple in the output.
20. Save the circuit before you close the program.[14]

- *What is your conclusion about the importance of the voltage regulator?*

[13] This surge is caused by the need of the capacitor for a high charging current.
[14] If you would like to save the circuit under a different name, go to File >> Save As, type the name, and then click OK.

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**VALUE**	**UNIT**
Repetitive peak reverse voltage		V_{RRM}	100	V
Reverse voltage		V_R	75	V
Peak forward surge current	t_p = 1 µs	I_{FSM}	2	A
Repetitive peak forward current		I_{FRM}	500	mA
Forward continuous current		I_F	300	mA
Average forward current	V_R = 0	$I_{F(AV)}$	150	mA
Power dissipation	l = 4 mm, T_L = 45 °C	P_{tot}	440	mW
	l = 4 mm, $T_L \leq$ 25 °C	P_{tot}	500	mW

Figure 5.3 Absolute Maximum Ratings for the 1N4148.

EXPERIMENT

6

Operational Amplifiers (Op Amps)

OBJECTIVES:

- To get acquainted with the essence of operation of the operational amplifier (op amp).
- To apply negative feedback on an op amp circuit to implement a noninverting amplifier that has a better-controlled closed-loop voltage gain.
- To use an op amp in its open-loop configuration as a comparator to sense light intensity change.

MATERIALS:

- Laboratory setup, including rastered socket panel
- One 741-type operational amplifier (op amp)
- 2 light emitting diodes (LEDs)
- Resistors (1 kΩ, 10 kΩ, 27 kΩ, 39 kΩ)
- 1 decade resistance box
- 1 light dependent resistor (LDR)
- Several wires and bridging plugs

INTRODUCTION

The operational amplifier is a versatile *integrated circuit* (IC) that performs various types of analog signal processing tasks. The most popular op amp is the μA 741 (Fig. 6.1), which was introduced by Fairchild in 1968 to become the industry standard.

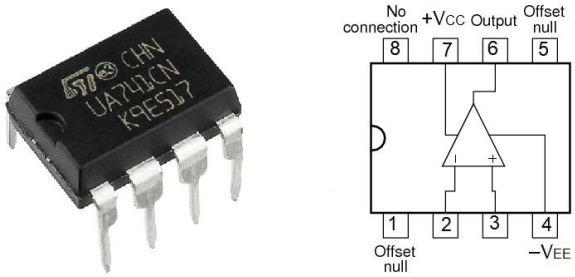
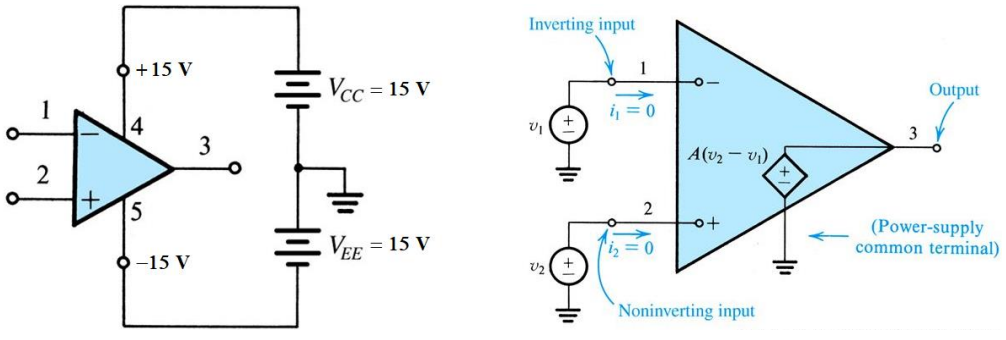


Figure 6.1 The popular μA 741 op amp IC package and its pin diagram.

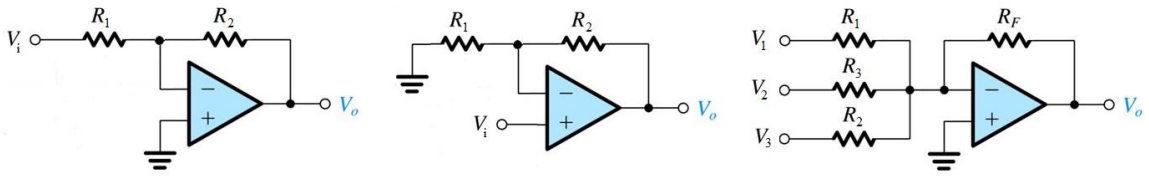
Figure 6.2a shows the circuit symbol of the op amp, along with its power connection scheme. Powering the op amp with bipolar dual power supplies is the common practice, but a single power supply powering may be used in special applications. The power supplies bias the internal transistors of the op amp, and provide power to the output load and the feedback network. However, these **power rails** put limits on the maximum and minimum swings of the output voltage. As long as an op amp output is not saturated at its power rails limits, it operates linearly with an equivalent circuit like the one shown in Fig. 6.2b.

As suggested by its idealized equivalent circuit, an op amp **amplifies the difference** between two input voltages and produces a **single-ended output**. It is characterized by a very large **open-loop gain** *A*, a very large input impedance, and a very small output impedance. A predictable **closed-loop gain** *G* can be obtained using **negative feedback**. The effect of negative feedback is to make the closed-loop gain almost entirely dependent on external components (e.g., R_1 and R_2). Presuming negative feedback and an ideal op amp, the analysis of op amp circuits can be greatly simplified by assuming that the two input terminals sit at the same potential (**virtual short**) and draw negligible current (**infinite input impedance**).



(a) (b)

Figure 6.2 (a) Circuit symbol and **(b)** equivalent circuit of the ideal op amp [1].



(a) (b) (c)

Figure 6.3 A variety of op amp circuits.

Figure 6.3 shows a variety of op amp circuits: (a) an **inverting amplifier**, (b) a **noninverting amplifier**, and (c) a **weighted summer**. Please refer to the textbook by Sedra and Smith for further details [1].

In the first part of this experiment we shall assemble and test a noninverting amplifier (Fig. 6.4a). In that circuit, since the noninverting terminal of the op amp draws negligible current (ideally zero), R_1 and R_2 are effectively in series; thus v_i and v_O are related by a simple voltage divider rule,

$$v_i = v_O \frac{R_1}{R_1 + R_2}$$

$$\rightarrow G \equiv \frac{v_o}{v_i} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R2}{R1} \qquad (6.1)$$

If no negative feedback is employed, an op amp is said to operate in the **open-loop** mode. In that mode, an op amp basically works as a comparator. If v_2 exceeds v_1 by few tens of microvolts, the output will saturate at an upper saturation level V_O^+ which is very close to and smaller than the positive rail voltage ($\approx V_{CC}$). If, however, v_1 exceeds v_2 by few tens of microvolts, the output will saturate at a lower saturation level V_O^- ($\approx -V_{EE}$).

A photocell, also called **L**ight **D**ependent **R**esistor(LDR), is a resistor whose resistance (R_{cell}) decreases with increasing incident light intensity. It is made of a high resistance semiconductor such as cadmium sulfide (CdS).

In the second part of this experiment we shall use such a resistor, along with an op-amp connected in an open-loop configuration, to detect changes in light intensity (Fig. 6.4b). In that circuit, a sufficiently small value of R_{cell}, which is a characteristic of the uncovered case, makes $V_2 > V_1$ by more than few tens of microvolts $\Rightarrow V_O = V_O^+ (\approx V_{CC})$ and consequently LED 1 conducts and glows. On the other hand, higher values of R_{cell}–the covered case– makes $V_1 > V_2$ by more than few tens of microvolts $\Rightarrow V_O = V_O^- (\approx -V_{EE})$ and consequently LED 2 conducts and glows.

PROCEDURE A

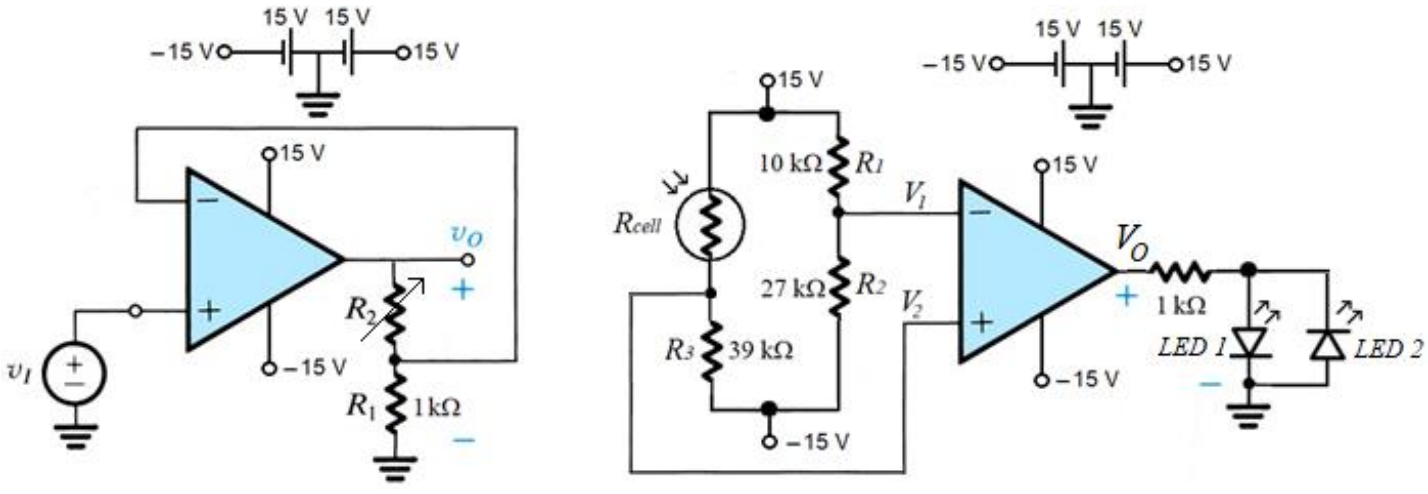
1. Construct the circuit shown in Fig. 6.4a; start off with a value of 10 kΩ for R_2.
2. Using a function generator, apply a 1-kHz, 1 $V_{pk\text{-}pk}$ sinusoid to the noninverting terminal of your op amp.
3. Using an oscillosccope, display $v_i(t)$ and $v_O(t)$ simulatenously (using the dual mode).
4. Record $v_i(t)$ and $v_O(t)$ on Fig. 6.5.
5. Measure and record the peak-to-peak value of the output and determine the closed-loop gain using:

$$G = \frac{V_{o(\text{pk-pk})}}{V_{i(\text{pk-pk})}} \qquad (6.2)$$

6. Now, using the decade box, increase R_2 gradually while observing how $v_O(t)$ amplitude changes. Record the maximum value of R_2 that will produce **unclipped** output.
7. Increase R_2 beyond that value (e.g., 40 kΩ) then display and sketch $v_i(t)$ and $v_O(t)$ on Fig. 6.6.
8. From the previous step, find $v_O(t)$ upper and lower limiting levels, V_O^+ and V_O^-.

PROCEDURE B

1. Using a DMM set to measure resistance, measure the resitance of a covered and uncovered photocell and record that in Table 6.2.
2. Assemble the circuit shown in Fig. 6.4b.
3. Using a DMM set to measure dc voltage, measure V_2, V_1, and V_O (with respect to ground).
4. Which LED is forward biased by V_O and consequently glows? Record your findings in Table 6.2.
5. Cover the photocell (LDR) and repeat the previous step.



(a) (b)

Figure 6.4 **(a)** The noninverting amplifier. **(b)** Comparator to sense light intensity change.

RESULTS

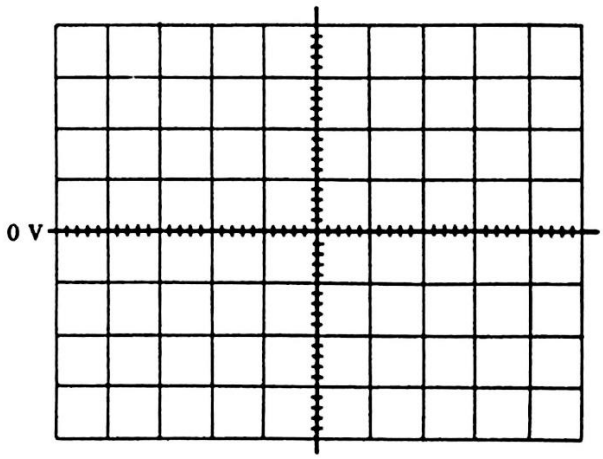


Figure 6.5

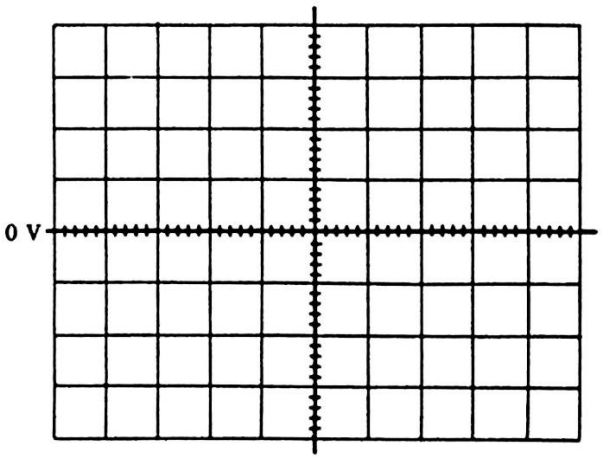


Figure 6.6

Table 6.1 Procedure A

R_2 value	Theoritical Gain (equation 1)	$V_{o(pk\text{-}pk)}$	Measued Gain = $V_{o(pk\text{-}pk)} / V_{i(pk\text{-}pk)}$
10 kΩ			
R_2 (max) =			
Limiting Levels			
V_O^+ =		V_O^- =	

Table 6.2 Procedure B

R_{cell} (uncovered):		R_{cell} (covered):		
case	V_2	V_1	V_O	which LED glows?
uncovered				
covered				

ASSIGNMENT 5

[CLO 3, CLO 4, CLO 5]

Using LTSpice, perform an AC analysis for different values of R_2 to see how changing the closed-loop gain G of a noninverting amplifier (Fig. 6.7) affects its bandwidth–the range of frequencies over which the gain remains within **0.707** (3 dB) of its maximum value.

Use 1 kΩ for R_1 and the following values for R_2: SN kΩ, (3×SN) kΩ, (5×SN) kΩ, (7×SN) kΩ, where SN stands for your serial number in your section. Use a frequency range from 1 Hz up to 10meg Hz. Measure the bandwidth for each value of resistance.

Summarize your findings in a table showing the value of G and the corresponding bandwidth for each value of resistance. Comment on the effect of increasing G on the bandwidth.

You need to include the circuit's schematic and the simulation results of your design in your assignment submission. To do that in LTspice, click on Tools >> Copy bitmap to Clipboard. Then paste the copied image in your Word document.

Watch the following video if you need help:

https://lms.ksu.edu.sa/bbcswebdav/users/talmadhi/EE312/LTSpice_HW5.mp4

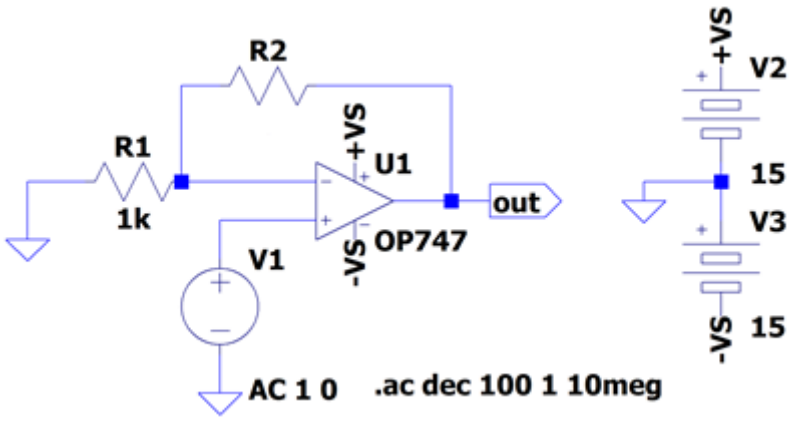


Figure 6.7

EXPERIMENT

7

Characteristics of the *n*-Channel MOSFET

OBJECTIVES:

- To be get acquainted with the basic principles of operation of the enhancement *n*-channel MOS transistor.
- To experimentally obtain the necessary measurements to plot the i_D-v_{DS} characteristics for a sample *n*-channel MOS transistor.
- To learn how to calculate important parameters from the experimentally-obtained data.

MATERIALS:

- Laboratory setup, including rastered socket panel
- One NMOS transistor (e.g., IRF620)
- 1 Resistor (1 kΩ)
- Several wires and bridging plugs

INTRODUCTION

There are two major types of three-terminal semiconductor devices: the MOSFET and the BJT, which we shall study in experiments 9 and 10. The basic principle involved in a three-terminal device is *the use of the voltage between two terminals to control the current flowing through the third terminal* [1].

In an *n*-channel enhancement-type MOSFET, the **gate**-to-**source** voltage, v_{GS}, controls the current flowing through the **drain**, i_D. The value of v_{GS} at which a conducting channel between the drain and the source is induced is called the threshold voltage, V_t. If $v_{GS} < V_t$, the device is said to be **cutoff**. If $v_{GS} > V_t$, however, the device could be either in **triode** or in **saturation**, depending on the value of v_{DS} compared to the gate-to-source overdrive voltage $v_{OV} \equiv v_{GS} - V_t$. In the triode and cutoff modes of operation, the MOS transistor is used mainly as an **electronic switch**. In the saturation mode, and for sufficiently small signals, the MOS transistor acts as a linear voltage-controlled current source, and consequently can be used as an **electronic amplifier**.

In the saturation mode of operation, i_D is related to v_{GS} and v_{DS} by

$$i_D = \frac{k_n'}{2}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \qquad (7.1)$$

To act as a good amplifier, a MOSFET has to have a high **transconducatnce**, g_m. At a constant v_{DS} in the saturation region, g_m quantifies how much the drain current changes for a small change in v_{GS}; thus

$$g_m \equiv \frac{\Delta i_D}{\Delta v_{GS}} = \frac{2I_D}{V_{GS} - V_t} \qquad (7.2)$$

The saturation mode is characterized by a weak dependence of i_D on v_{DS} and a much greater dependence on v_{GS}. Caused by a phenomenon known as **channel-length modulation**, the weak dependence of i_D on v_{DS} –in the saturation region–at a constant V_{GS} is linear, and can be modeled by a finite resistance[15] r_o between the drain and the source, which is given by

$$r_o \equiv \frac{\Delta v_{DS}}{\Delta i_D} = \frac{1}{\lambda I_D} \qquad (7.3)$$

where I_D is the drain current without channel length modulation (at edge of saturation).

In the triode region, and for small v_{DS}, the MOS transistor effectively acts as a voltage-controlled resistance. Its **closure resistance**[16] (while acting as a closed switch) r_{DS} is given by

$$r_{DS} \equiv \frac{\Delta v_{DS}}{\Delta i_D} = \frac{1}{k_n' \frac{W}{L} V_{OV}} \qquad (7.4)$$

[15] This resistance is important in assessing how effective a MOSFET will be if used in an amplifier circuit.
[16] This resistance is important in assessing how effective a MOSFET will be if used in switching applications.

PROCEDURE A: Measuring V_t

1. Assemble the circuit shown in Fig. 7.1a.
2. Using a variable dc power supply, increase V_{DD} until V_{1k} becomes 0.25V (250 mV), which translates to a drain current 250 μA. This roughly will mark the onset of strong inversion for this particular transistor only, the IRF620[17], according to its datasheet.
3. Using a DMM, measure and record the value of V_{GS}. This value of V_{GS} will *approximately* be equal to the threshold voltage, V_t.

V_t =

PROCEDURE B: Obtaining The Terminal Characteristics

1. Construct the circuit shown in Fig. 7.1b.
2. Using one dc power supply, set and fix V_{GS} at ($V_{GS1} = Vt + 0.2$); use the V_t value that you have just measured in procedure A. *Verify this value using a DMM.*

3. Using another dc power supply, vary V_{DD} to obtain the V_{DS} values shown in Table 7.1. For each value of V_{DS}, measure and record V_{RD}. *The corresponding values of I_D can be found from Ohm's law.*

4. Turn off the dc power supplies for two minutes to let the transistor cool down, turn them on again, and then increase V_{GS} by 0.1 V; that is, $V_{GS2} = V_t + 0.3$; *verify this value using a DMM*. Repeat step 3 while keeping the supply V_{GS} fixed at V_{GS2}.

5. Turn off the dc power supplies for two minutes to let the transistor cool down, turn them on again, and then increase V_{GS} by another 0.1 V; that is, $V_{GS3} = V_t + 0.4$; *verify this value using a DMM*. Redo step 3 while keeping the supply V_{GS} fixed at V_{GS3}.

6. Based on your measurements:
   a. Use MATLAB® (see Appendix B) to plot i_D (mA) vs. v_{DS} (V) for each value of v_{GS}. Label each curve with the corresponding values of v_{GS}. Label the three regions of operation on your graph.
   b. Using $r_o \equiv \frac{\Delta v_{DS}}{\Delta i_D}$, calculate r_o for $V_{OV} = 0.3$ V, $V_{DS1} = 1$ V and $V_{DS2} = 5$ V.
   c. Using the above value of r_o, and knowing I_D at $V_{DS} = V_{OV}$, calculate λ.
   d. Using $r_{DS} \equiv \frac{\Delta v_{DS}}{\Delta i_D}$, calculate r_{DS} for $V_{OV} = 0.3$ V, $V_{DS1} = 0$ V and $V_{DS2} = 0.05$ V.

[17] The IRF620, is a discrete **power MOSFET** whose typical threshold voltage is around 3 V (see Appendix C), which is relatively large compared to MOSFETs fabricated on an Integrated Circuit (IC).

RESULTS

Table 7.1

$V_{GS1} = V_t + 0.2$ V (**V_{OV} = 0.2**)			$V_{GS2} = V_t + 0.3$ V (**V_{OV} = 0.3**)			$V_{GS3} = V_t + 0.4$ V (**V_{OV} = 0.4**)		
V_{DS} (V)	V_{RD} (V)	I_D (mA)	V_{DS} (V)	V_{RD} (V)	I_D (mA)	V_{DS} (V)	V_{RD} (V)	I_D (mA)
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05			0.05			0.05		
0.10			0.10			0.10		
0.20			0.20			0.20		
0.30			0.30			0.30		
0.40			0.40			0.40		
0.50			0.50			0.50		
1.00			1.00			1.00		
5.00			5.00			5.00		

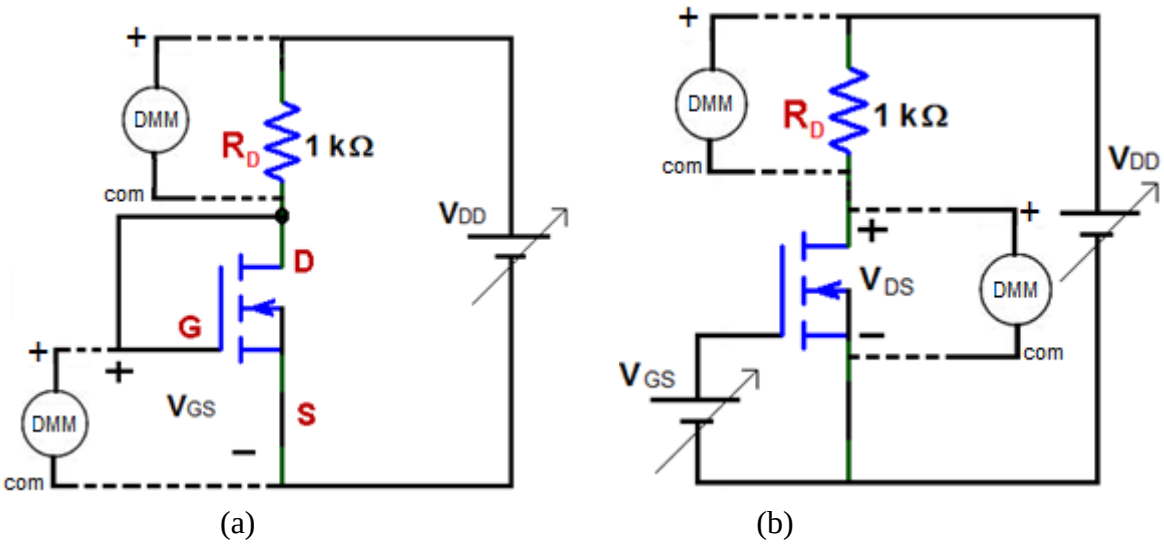


Figure 7.1 Circuit setup for measuring: **(a)** the threshold voltage, **(b)** the i_D-v_{DS} characteristics.

EXPERIMENT

8

Simulation of MOS Logic Inverter Circuits

OBJECTIVES:

- To use a software tool, like LTspice®, to obtain and examine the voltage transfer characteristics (VTC) and the dynamic responses for the:
    - Resistive-load logic inverter, which is basically a common-source circuit.
    - CMOS inverter.
- To explore, with aid of simulation, some factors that affect the dynamic response performance for both circuits.

MATERIALS:

- A PC or a laptop with LTspice® installed
-
- A flash memory to save your work for future reference and further study.

INTRODUCTION

Figure 8.1 shows how a logic inverter can be implemented using a voltage-controlled switch. When v_I is low (logic 0), the switch will be open and no current flows in the circuit; therefore, $v_O = V_{DD}$ (logic 1). On the other hand, when v_I becomes high enough to close the switch, current flows in the circuit and v_O will be low (logic 0) due to the closure resistance R_{on} of the switch being significantly lower than R.

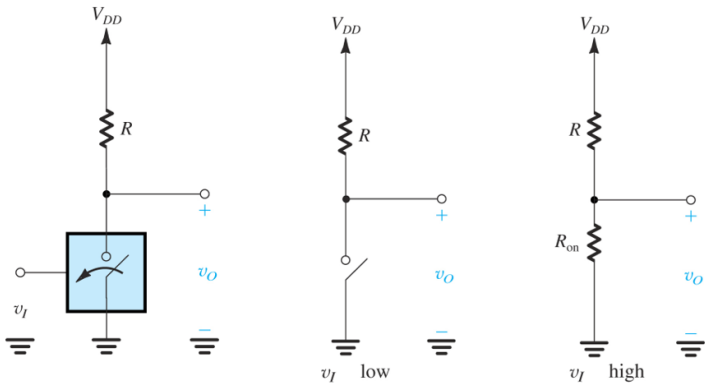


Figure 8.1 Implementing a logic inverter using a resistor and an electronic switch [1].

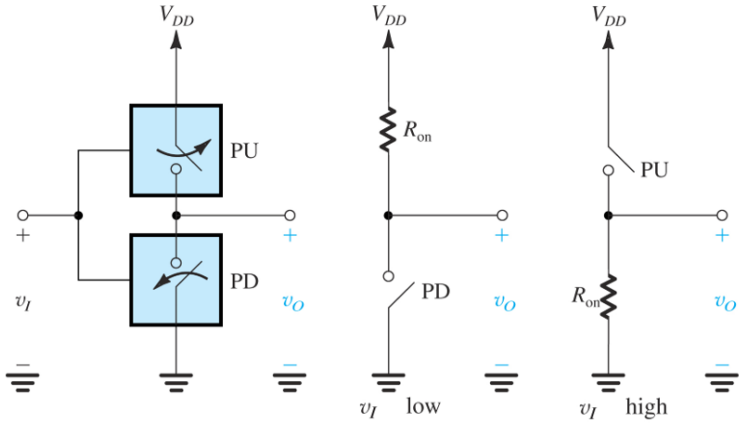
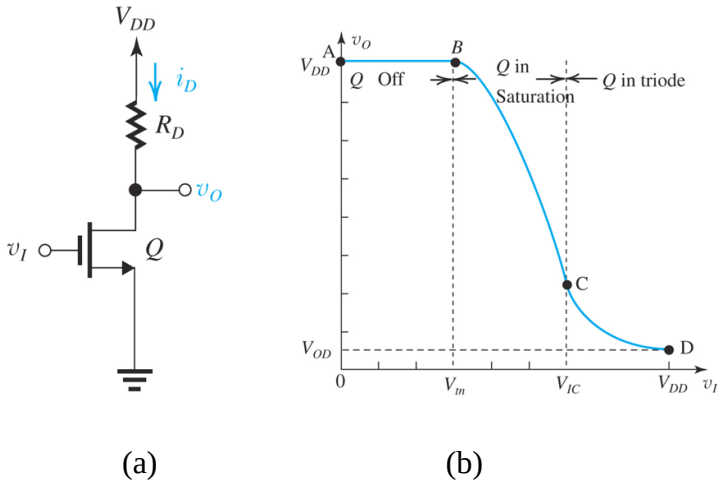


Figure 8.2 Implementing a logic inverter using two complementary electronic switches [1].

Figure 8.2, on the other hand, shows how a logic inverter can be better implemented using two *complementary* voltage-controlled switches. When v_I is low (logic 0), the pull-down (PD) switch will be open and the pull-up (PU) switch closed; therefore, the output node will be pulled up to V_{DD} (logic 1) through a very low resistance R_{on}. On the other hand, when v_I is high (logic 1), the PD switch will be closed and the PU switch open; therefore, the output will be pulled down to ground (logic 0) through R_{on}.

The **Resistive-load inverter** (Fig. 8.3a.), which is basically **a common-source** (CS) circuit, can be used to implement the one-switch logic inverter. In such a circuit, an MOS transistor is employed as voltage-controlled switch. The voltage transfer characteristic of this circuit is shown in Figure 8.3b [1]. The VTC has two extreme regions, where the circuit can be used as a digital logic inverter, and a transition region in the middle where the circuit can be used as an inverting amplifier. For $v_I < V_t$ (segment A to B), the MOS transistor is cut off; hence acting as an **open switch**. For $v_I \geq V_t$ and less than V_{IC} (segment B to C), v_{GD} is less

than V_t ; therefore, the MOSFET is saturated, and the circuit can be used to **amplify** a small signal riding over an appropriate dc offset voltage. For $v_I \geq V_{IB}$ (segment B to C), the MOS transistor operates at $v_{GD} > V_t$, which is a characteristic of the triode region; hence the device is effectively acting as a **closed switch** with a voltage-dependent closure resistance, r_{DS}.



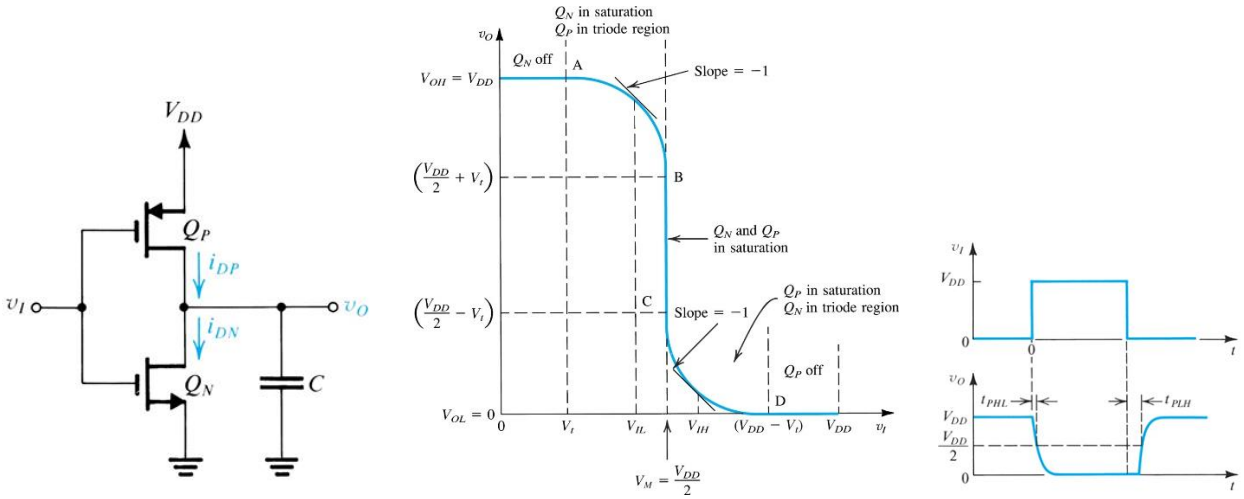
(a) (b)

Figure 8.3 **(a)** The CS circuit and **(b)** its transfer characteristic [1].

On the other hand, the two complementary switches based logic inverter shown in Fig. 8.2 can naturally be implemented by the **CMOS** inverter (Fig. 8.4a). In a CMOS inverter circuit, an NMOS transistor is used as a PD switch, while a PMOS device is used as complementary PU switch. The voltage transfer characteristic of this circuit is shown in Figure 8.4b [1]. The most distinctive feature of this circuit is that the two complementary MOS transistors are not turned on simultaneously– making it possible for the circuit to have very minimized (ideally zero) static power dissipation.

Figure 8.4c shows the dynamic response of the CMOS inverter. Evidently, there is a **propagation delay** between the two waveforms due the nonzero switching time of the transistor, which is strongly dependent on its *W/L* ratio. Furthermore, there is capacitance that is inevitably present between the output node and ground due to wiring and device parasitic capacitances. The propagation delay is approximately equal to $0.7 \times R_{on(avg)} \times C$, where $R_{on(avg)}$ is the **average switching resistance** of the MOS transistor, which is proportional to (*L/W*) of the transistor.

To have equal propagation delays, an inverter has to have a matched MOS transistors pair; that is, $W_p = (\mu_n/\mu_p)\, W_n \approx 3W_n$. If two MOS transistors are needed to be connected in series, as in the PD network of a NAND gate or the PU network of a NOR gate, the individual widths have to doubled.



(a) (b) (c)

Figure 8.4 **(a)** The CMOS inverter, **(b)** its transfer characteristic, and **(c)** its dynamic response. [1].

PROCEDURE A: The Common Source Circuit

1. Download the following file:[18]
   https://lms.ksu.edu.sa/bbcswebdav/users/talmadhi/mosfet1u.lib
2. Save it under this folder: Documents\LTspiceXVII\lib\cmb
3. Double click the LTspice icon on the desktop.
4. Go to File >> New Schematic.

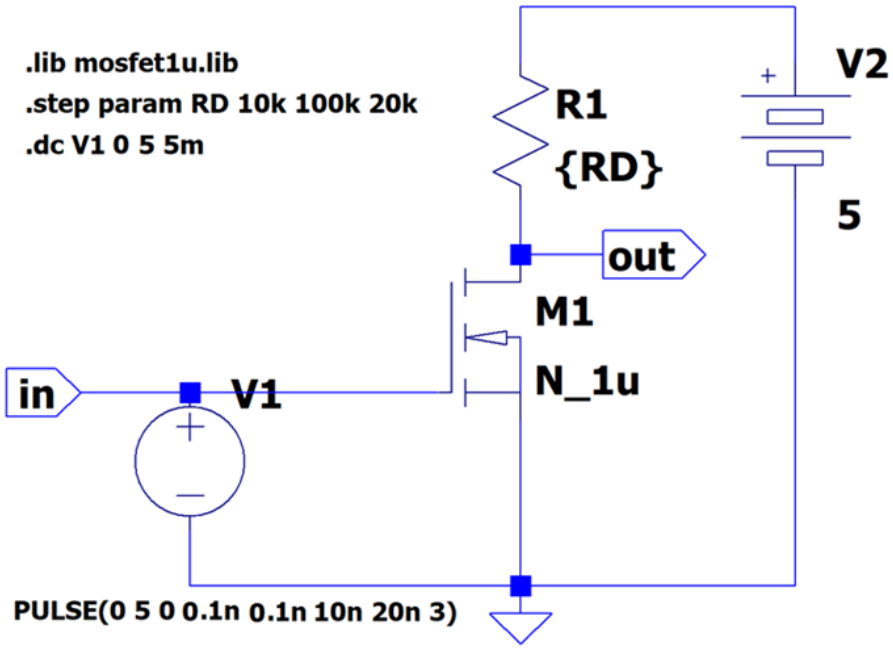


Figure 8.5 Implementing the CS circuit in LTspice.

5. Place all of the components required to build the circuit of Fig. 8.5 on your schematic. To obtain the N_1u MOSFET, add an nmos4 component, then right-click on the NMOS default name and change it to N_1u.
6. Wire all components, add a ground (GND), and label the **in** and **out** nodes.
7. To add the **.lib** and **.step** commands, go to Edit >> .op SPICE directive'S', or just press the 'S' key, then type the .lib command as shown in Fig. 8.5, then press Ctrl+M and type the .step command.
8. To adjust the voltage source V1 parameters, right click on it, then select *Advanced*, and then select PULSE. Fill in the required fields, which are: (Vinitail = 0, Von = 5, Tdelay = 0, Trise = 0.1n, Tfall = 0.1n, Ton = 10n, Tperiod = 20n, Ncycles = 3).
9. To add a DC sweep command (**.dc**),[19] go to Edit >> SPICE analysis, and then fill in the required fields, which are: (Name of 1st source to sweep = V1, Type of sweep = Linear, Start value = 0, Stop value = 5, Increment = 5m), then click OK.
10. To run your simulation, go to Simulate >> run, or just click on the run icon.
11. Place the mouse pointer on the out node on the schematic, and then make a left click to see the VTC curves of the circuit.

[18] This file contains the SPICE models of a 1-μm (minimum channel length) process.
[19] In order to obtain the voltage transfer characteristic (VTC) of the circuit.

- *How does the value of R_D in the transition region affect the magnitude of the slope, and hence the voltage gain of the circuit?*
- *How does the value of R_D affect output low level V_{OL}?*

We will now do a transient analysis to see the dynamic response of the circuit.

12. Go to Edit >> SPICE analysis, click on the Transient tab, and then fill in the required fields, which are:
(Stop time = 60n[20] , Time to start saving data = 0, Maximum Timestep = 0.01n).
13. Click on the run icon.
14. Place the mouse pointer on the **out** node on the schematic, and then make a left click by the mouse to see the output voltage waveforms.
15. Place the mouse pointer on the **in** node on the schematic, and then make a left click to see the input voltage waveform.
    - *Which logic gate does the circuit implement?*
16. Use the mouse to zoom in (click and drag to draw a rectangular box) around the transition area, where the input falls and the output waveforms rise)
    - *Which value of R_D corresponds to maximum propagation delay?*
    - *Summarize the effect of R_D on the circuit performance if used as an amplifier and if used as a logic inverter (NOT gate).*
17. Save your circuit by pressing Ctrl+S.

PROCEDURE B: The CMOS Inverter

1. Go to File >> New Schematic.

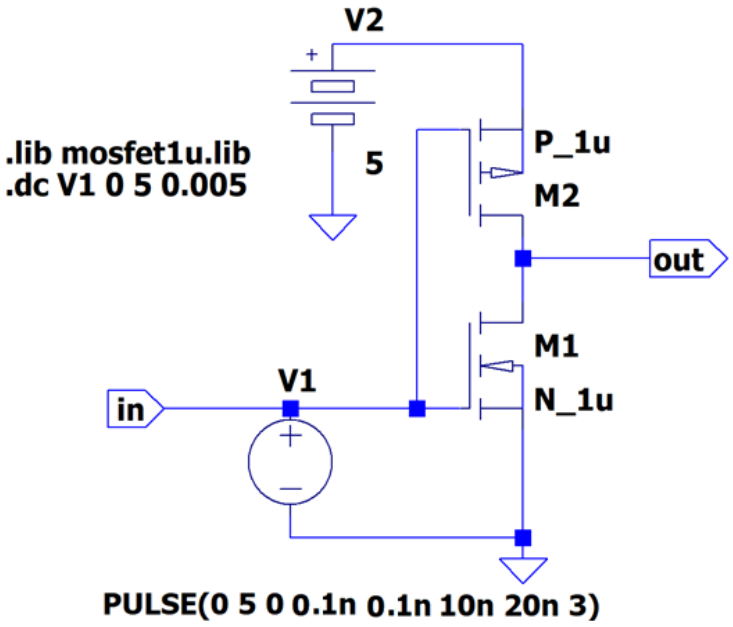


Figure 8.6 Implementing the CMOS inverter (NOT gate) in LTspice.

[20] This can be found by multiplying Tperiod by Ncycles.

2. Place all of the components required to build the circuit of Fig. 8.6 on your schematic. To obtain the N_1u MOSFET, add an nmos4 component, then righ-click on the NMOS default name and change it to N_1u. To obtain the P_1u MOSFET, add pmos4 component, then right-click on the PMOS default name and change it to P_1u.
3. Wire all components, add a ground (GND), and label the **in** and **out** nodes.
4. Adjust V1 as you have done in procedure A.
5. Add the **.lib** command as you have done in procedure A.
6. Add the **.dc** command as you have done in procedure A.
7. Click on the run icon.
8. Place the mouse pointer on the out node on the schematic, and then make a left click to see the VTC curve of the circuit.

We will now do a transient analysis to see the dynamic response of the circuit.

9. Go to Edit >> SPICE analysis, click on the Transient tab, and then fill in the required fields, which are:
   (Stop time = 60n, Time to start saving data = 0, Maximum Timestep = 0.01n).
10. Click on the run icon.
11. Place the mouse pointer on the **out** node on the schematic, and then make a left click by the mouse to see the output voltage waveforms.
12. Place the mouse pointer on the **in** node on the schematic, and then make a left click to see the input voltage waveform.
    - *Which logic gate does the circuit implement?*
13. Use the mouse to zoom in (click and drag to draw a rectangular box) around the transition area, where the input falls and the output waveforms rise)
    - *What is the propagation delay for this gate?*
14. Save your circuit by pressing Ctrl+S.

ASSIGNMENT 6

[CLO 3, CLO 4, CLO 5]

1. Do an LTspice transient analysis of the circuit shown in Fig. 8.7. Measure the propagation delay between *V(in)* and *V(out)*, and the propagation delay between *V(in)* and *V(inv1_out)*.
2. What is your observation regarding the propagation delay of the output voltage waveform of the third inverter *V(out)* compared to that of the first inverter *V(inv1_out)*?
3. Do an LTspice transient analysis of the circuit shown in Fig. 8.8.
4. After simulating the circuit, examine at the *V(X)*, *V(Y)*, and *V(out)* waveforms. Find the truth table.[21]
    - *What logic gate does this circuit implement?*
5. Try to justify the truth table you have obtained based on your understanding of how complementary switches (PMOS and NMOS transistors) work.

    Hint: A high input voltage activates an NMOS transistor (effectively making its channel resistance very low, hence serving as a closed switch). In contrast, a low input voltage activates a PMOS transistor (effectively making its channel resistance very low, hence serving as a closed switch). The output node either gets pulled up to high voltage level or pulled down to ground (low voltage level) depending on the existence of a closed switch (conducting path) between it and either VDD or ground.

You need to include the circuit's schematic and the simulation results of your design in your assignment submission. To do that in LTspice, click on Tools >> Copy bitmap to Clipboard. Then paste the copied image in your Word document.

[21] Consider the five-volt voltage level as a logic 1 and the zero-volt voltage level as a logic 0.

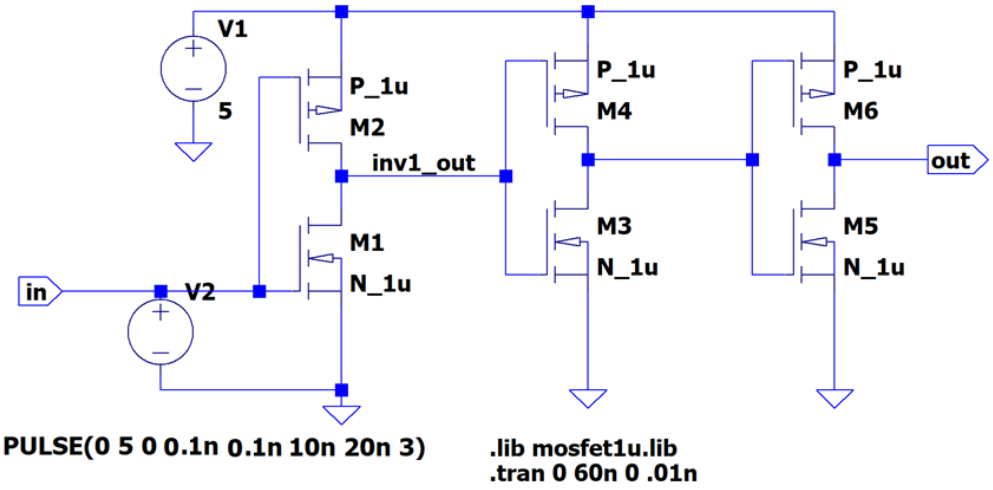


Figure 8.7 A circuit to explore the effect of cascading on propagation delay.

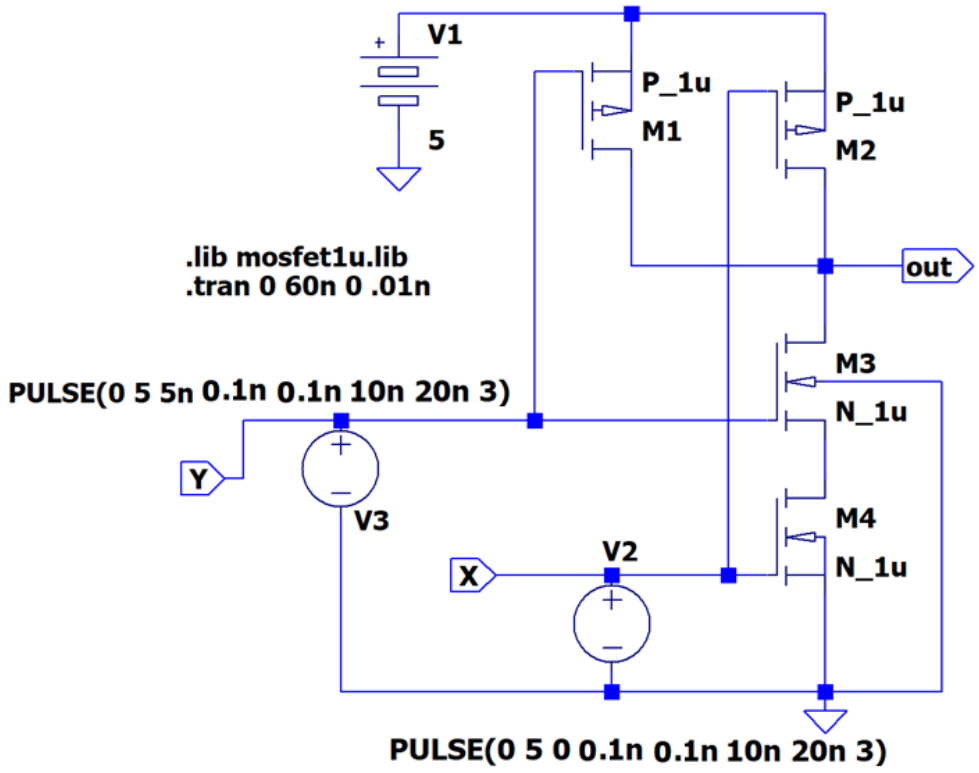


Figure 8.8

EXPERIMENT

9

Introduction to The BJT
The Common Emitter Circuit

OBJECTIVES:

- To experimentally obtain and carefully examine the voltage transfer characteristic (VTC) of a simple common-emitter (grounded emitter) circuit.
- To discuss and understand the implications of the VTC of that circuit on using it as either a common-emitter amplifier or as a resistive-load inverter.
- To learn a practical technique for designing a dc biasing scheme that will produce a stable Q point despite any potential variations in temperature and/or β.

MATERIALS:

- Laboratory setup, including rastered socket panel
- One *npn* BJT transistor (e.g., BD137)
- Resistors (27 kΩ, 2.7 kΩ)
- Several wires and bridging plugs

INTRODUCTION

The BJT is the second three-terminal device we encounter in this course. Despite the fierce competition with the MOSFET, the BJT is more popular in discrete-circuit design. Moreover, because of its reliable performance in sever environmental conditions, it is *the* dominant device in automotive applications [1]. Radio frequency (RF) circuits, and very high-speed digital circuits are two other fields where BJTs excel. Manufacturers generally classify their BJTs into three broad categories: general-purpose/small signal devices, power devices, and RF (radio frequency/microwave) devices [3].

There are two types of BJTs: the *npn* transistor and its dual, the *pnp* transistor. In this experiment we are going to concentrate on the *npn* type, with the BD137 as an example. One example of a BD137 datasheet is provided in Appendix C for easy reference, but one can always go online to search for datasheets for any particular device.

The three terminals of the BJT are connected to three semiconductor layers: the **emitter** (E), the **base** (B), and the **collector** (C). As such, it consists of two *pn* junctions, the emitter-base junction (**EBJ**) and the collector-base junction (**CBJ**). Based on the bias condition of these two junctions, three distinct modes of operation are obtained, as shown in Table 9.1. The **cutoff mode** and the **saturation mode** are employed in switching applications (e.g., logic circuits). The **active mode** is the one used if the transistor is to operate as a linear amplifier.

Since a BJT has two pn junctions, it can be tested by a DMM set to its diode-test mode. Both junction should read about 0.6 V when forward-biased and an OL when reverse-biased. If a DMM is connected between the collector and emitter, it should read OL.

Figure 9.1 shows the voltage polarities and current flow directions for an *npn* transistor biased to operate in the active mode. The base of a BJT does a similar role to the gate of a MOSFET, except that it does need a dc current in order for the BJT to function properly. Consequently, the emitter current I_E is not equal to the collector current I_C, as the difference between them equals the base current I_B according to Kirchhoff's current law. In the active mode of operation, I_C is directly proportional to I_E via the **common-base current gain** α, and directly proportional to I_B via the **common-emitter current gain** β, which is usually denoted $\mathbf{h_{FE}}$ in datasheets.

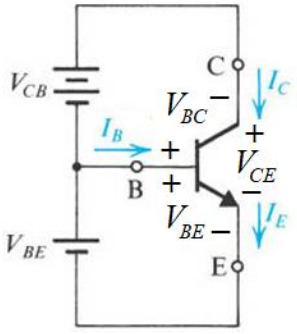


Figure 9.1 Voltage polarities and current flow for an *npn* transistor.

Table 9.1

Mode	EBJ bias condition	CBJ bias condition
Cutoff	$v_{BE} < V_{BE\,on} \approx 0.5$ V $\Rightarrow$ reverse/slightly-forward	$v_{BC} < V_{BC\,on} \approx 0.4$ V $\Rightarrow$ reverse/slightly-forward
Active	$v_{BE} \geq V_{BE\,on} \approx 0.5$ V $\Rightarrow$ forward	$v_{BC} \leq V_{BC\,on} \approx 0.4$ V $\Rightarrow$ reverse/slightly-forward
Saturation	$v_{BE} \geq V_{BE\,on} \approx 0.5$ V $\Rightarrow$ forward	$v_{BC} > V_{BC\,on} \approx 0.4$ V $\Rightarrow$ forward
General Relationships: $I_E = I_B + I_C$		$V_{BC} = V_{BE} - V_{CE}$
In the **active** mode: $v_{CE} > 0.2$ V ; $\beta \equiv I_C / I_B$; $\alpha \equiv I_C / I_E$; $\alpha = \beta / (\beta+1)$		
In the **saturation** mode: $v_{CE} = V_{CE\,sat} = 0.1 – 0.2$ V ; $\beta_{forced} \equiv I_{Csat} / I_B$		

PROCEDURE

1. Assemble the circuit shown in Fig. 9.2.
2. Using one dc supply, fix V_{CC} at 5 V; using another dc supply, vary V_I to obtain V_O values that are shown in Table 9.2. For each value of V_O, measure V_{BE} and V_I and record their values in the table.
3. Do the required calculations in Table 9.2 using the following equations

$$I_B = (V_I – V_{BE})/R_B \qquad (9.1)$$

$$I_C = (V_{CC} – V_O)/R_C \qquad (9.2)$$

4. Plot the dc transfer characteristic (v_{OUT} $vs.$ v_{IN}) on the graph of Fig. 9.3.
5. Which region of the CE circuit transfer characteristic can be used for voltage amplification? Why?
6. Look at Table 9.2, then determine which current begins to saturate I_E, I_B or I_C as the operating point of the BJT moves into saturation.
7. From Table 9.2, calculate the voltage gains $G_V = \Delta v_O / \Delta v_I$ and $A_V = \Delta v_O / \Delta v_{BE}$ when v_O changes from 3.5 to 2.5 V. Why is $|G_V|$ usually less than $|A_V|$?
8. From Table 9.2,
   a. Calculate β at $v_O = 2.5$ V (in the active mode).
   b. Calculate β_{forced} at $v_O = 0.1$ V (in the saturation mode, β is denoted by β_{forced}, and it measures how deeply the BJT is saturated).

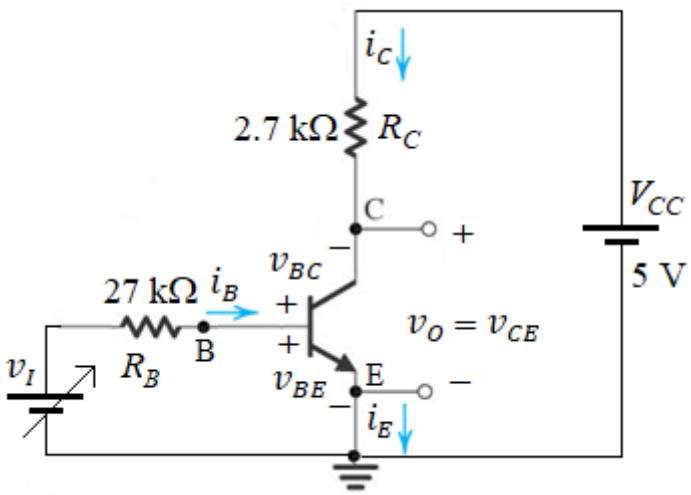


Figure 9.2 The Common Emitter Circuit.

RESULTS

Table 9.2 Measured Data (Rounded Up to 3 Decimal Places)

Vary V_I to obtain ↓	To be Measured		To be calculated				
$V_{CE} = V_O$ (V)	V_{BE} (V)	V_I (V)	$V_{BC} = V_{BE} - V_{CE}$ (V)	Mode of operation	I_B (mA)	I_C (mA)	I_E (mA)
5.000	0.000	0.000	-5.000	Cutoff	0.000	0.000	0.000
4.950							
4.500							
3.500							
2.500							
2.000							
1.500							
0.500							
0.200							
0.100							

Figure 9.3 VTC of the CE Circuit.

DISCRETE AMPLIFIERS BIAS SCHEMES

DESIGN TIPS

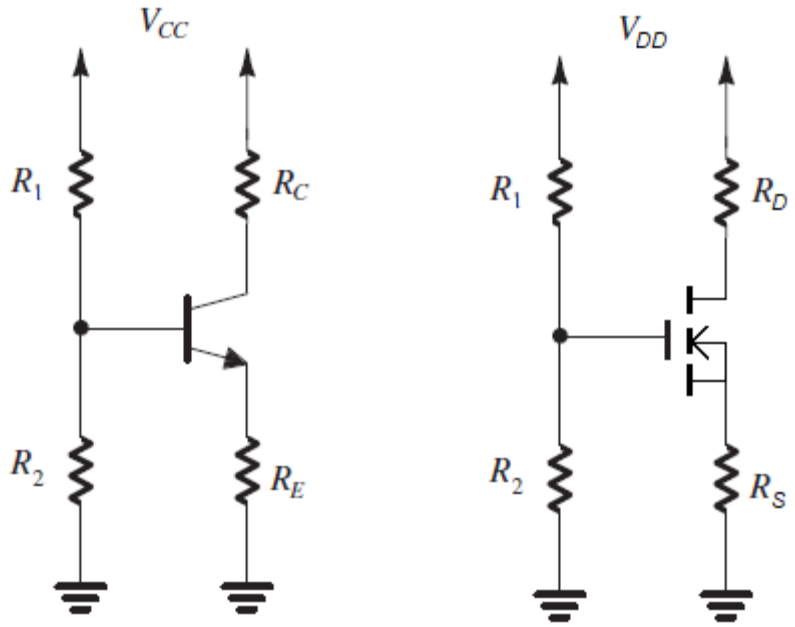
Discrete Common Emitter Amplifier Biasing Scheme

If common-emitter configuration is to be utilized in an amplifier circuit, a proper bias scheme to ensure a stable operating point in the active mode should be used. A classical discrete-circuit bias arrangement for the BJT is shown in Fig. 9.4a. It is the most commonly used scheme if a single power supply is available to the designer. It utilizes a voltage divider between two resistors, R_1 and R_2, to establish an appropriate voltage at the base to put the transistor in the active mode. We shall use such a biasing scheme to implement a common-emitter amplifier in experiment (10).

It is highly desirable to select the values of the bias resistors in such a way to make the operating point Q (I_{CQ}, V_{CEQ}) not strongly dependent on V_{BE} and β which vary with temperature and across samples of a given transistor type.

Starting off with a $V_{BE(on)}$ of 0.7 V and a known value of β, and for a given I_E (based on power budget), a proposed sizing scheme of the resistors goes like this:

- Start with $V_E = (1/3)\ V_{CC} \Rightarrow$ calculate R_E from Ohm's law.
- Select $R_C = R_E$ (*note*: for large β, $I_C \approx I_E$).
- Calculate $V_B = V_{BE(on)} + V_E$ and $I_B = I_E/(\beta+1)$
- Take I_2 to be at least $10I_B \Rightarrow$ calculate R_2 from Ohm's law ($V_{[across\ R2]} = V_B$).
- Given that $I_1 = I_B + I_2 = 11\ I_B$, calculate R_1 from Ohm's law ($V_{[across\ R1]} = V_{CC} - V_B$).
- Use Appendix F to find the nearest standard resistors to those you have calculated above.



(a) (b)

Figure 9.4 Classical discrete amplifiers bias arrangements.

Discrete Common Source Amplifier Biasing Scheme

If common-source configuration is to be utilized in an amplifier circuit, a proper bias scheme to ensure a stable operating point in the saturation mode should be used. A classical discrete-circuit bias arrangement for the MOSFET is shown in Fig. 9.4b. It is the most commonly used scheme if a single power supply is available to the designer. It utilizes a voltage divider between two resistors, R_1 and R_2, to establish an appropriate voltage at the gate to put the transistor in the saturation mode.

It is highly desirable to select the values of the bias resistors in such a way to make the operating point Q (I_{DQ}, V_{DSQ}) not strongly dependent on V_t and $k_n'W/L$ which vary with temperature and across samples of a given transistor type.

Starting off with a known value of $k_n'W/L$ and V_t, and for a given I_D (based on power budget) and a given $I_G = I_{G1} = I_{G2}$ (preferably in the μA range), a proposed sizing scheme of the resistors goes like this:

- Start with $V_S = (1/3)\ V_{DD} \Rightarrow$ calculate R_S from Ohm's law.
- Select $R_D = R_S$ (*note*: $I_S = I_D$).
- Calculate $V_G = V_{GS} + V_S$, where $V_{GS} = V_t + V_{OV}$, and $V_{OV} = \text{sqrt}(2I_D / k_n'W/L)$
- Knowing $I_{G2} = I_G$, and V_G, calculate R_2 from Ohm's law ($V_{[across\ R2]} = V_G$).
- Knowing $I_{G1} = I_G$, and V_G, calculate R_1 from Ohm's law ($V_{[across\ R1]} = V_{DD} - V_G$).
- Use Appendix F to find the nearest standard resistors to those you have calculated

ASSIGNMENT 7

[CLO 3, CLO 4, CLO 5]

1. Using the bias scheme design tips, and assuming V_{CC} = 9 V, $V_{BE(on)}$ = 0.7 V and a β of 120 in the circuit of Fig. 9.10, specify standard 5% resistors (Appendix F) to bias the BJT at I_E = SN mA, where SN is your serial number in your section.
2. Using the bias scheme design tips, and assuming V_{DD} = 15 V, V_t = 1.6 V and a k_n'W/L of 0.17 A/V^2 in the circuit of Fig. 9.11, specify standard 5% resistors (Appendix F) to bias the MOSFET at I_D = SN mA and I_D = SN μA, where SN is your serial number in your section.
3. Verify your designs using LTspice. In your simulation, change the default BJT to BCW60A for the BJT circuit and the default MOSFET to 2N7002 for the MOSFET circuit. You need to include the circuit's schematic and the simulation results of your design in your assignment submission. To do that in LTspice, click on Tools >> Copy bitmap to Clipboard. Then paste the copied image in your Word document.

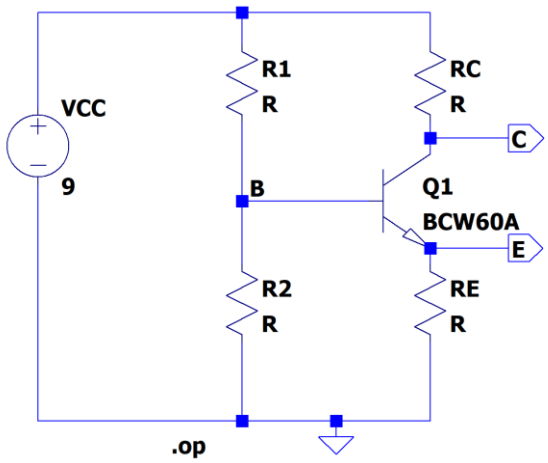


Figure 9.10 A single supply biasing of a BJT amplifier circuit.

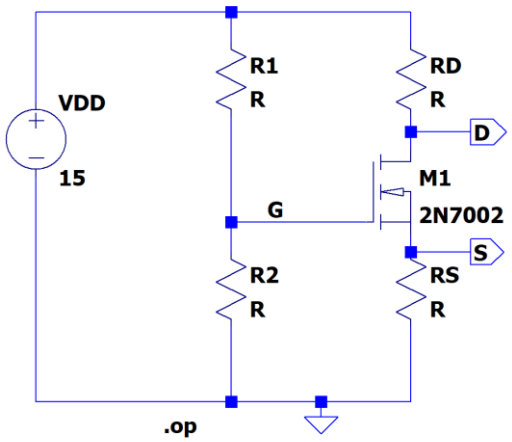


Figure 9.11 A single supply biasing of a MOSFET amplifier circuit.

EXPERIMENT

10

The Common Emitter Amplifier

OBJECTIVES:

- To assemble a common emitter amplifier circuit, perform dc and small signal measurements, and calculate some important parameters.
- To experimentally see the necessity of maintaining the input signal small enough to avoid output voltage distortion

MATERIALS:

- Laboratory setup, including rastered socket panel
- One *npn* BJT transistor (e.g., BD137)
- Resistors (4.7 kΩ, 5.6 kΩ, 27 kΩ, 47 kΩ)
- Electrolytic capacitors (2.2 μF (two), 470 μF)
- Several wires and bridging plugs

INTRODUCTION

The Common emitter (CE) amplifier is the most famous of the three BJT amplifier configurations. The other two being the common base (used to achieve higher bandwidth) and the common collector (used as a voltage buffer). The discrete CE amplifier receives the input signal at the base (via a coupling capacitor) and delivers the output from the collector.

Figure 10.1a shows only the dc circuit of such an amplifier. The dc bias scheme used here is known as the voltage divider bias with emitter degeneration resistance R_E. R_E serves to stabilize the dc bias point against variations in β. Moreover, including R_E increases the amplifier's input impedance, and extends its linear range. However, the presence of R_E reduces the transconductance g_m by a factor of $(1 + g_m R_E)$, hence reducing the voltage gain by the same factor. Shown in Fig. 10.1b is the complete CE amplifier circuit. Capacitors C_{C1} and C_{C2}, known as **coupling** capacitors, are used to act as a short circuit at signal frequencies of interest while blocking dc–hence, the other common name **dc-blocking** capacitors. A **bypass** capacitor, C_E, is used in order to bypass R_E at signal frequencies; therefore, nearly eliminate its undesirable effect on A_v. The CE amplifier is characterized by a 180° phase shift; it's an indication of the inverse relationship (negative slope) between its input and output as you may recall from experiment 9.

With **efficiently bypassed R_E**, the theoretical voltage gains of the CE amplifier are given by the following expressions [1]:

$$G_v \equiv \frac{v_o}{v_{sig}} = -g_m(R_C \parallel r_o \parallel R_L)\left\{\frac{R_1 \parallel R_2 \parallel (\beta+1)r_e}{R_{sig} + [R_1 \parallel R_2 \parallel (\beta+1)r_e]}\right\} \qquad (10.1)$$

$$A_v \equiv \frac{v_o}{v_i} = -g_m(R_C \parallel r_o \parallel R_L) \approx -g_m R_C \quad if\ R_C \ll r_o \parallel R_L \qquad (10.2)$$

$$A_v \approx -\alpha\frac{R_C}{r_e} = -\frac{I_C R_C}{V_T} \qquad (10.3)$$

$$g_m = \frac{I_C}{V_T} \quad and \quad r_e = \frac{V_T}{I_E} \qquad (10.4, 10.5)^{22}$$

Note that, in contrast to the common source (CS) MOSFET amplifier, R_{sig} of the input source affects the overall voltage gain–because, at low frequencies, the input resistance of a CE amplifier is much smaller than that of a CS amplifier.

Refer to the datasheet of the BD137 transistor given on Appendix C. Note that the maximum allowable V_{CE} is 60 V, and the maximum allowable power dissipation P_D at an ambient temperature T_A of 25 °C is 1.25 W. That value should be derated for higher ambient temperatures using the following simple equation:

$$P_D|_{higher\ temp} = P_D|_{at\ 25\,^\circ C} - DF \times (higher\ temp - 25) \qquad (10.6)$$

where the power derating factor *DF* at T_A = 25 °C is 10 mV/°C as given in the datasheet.

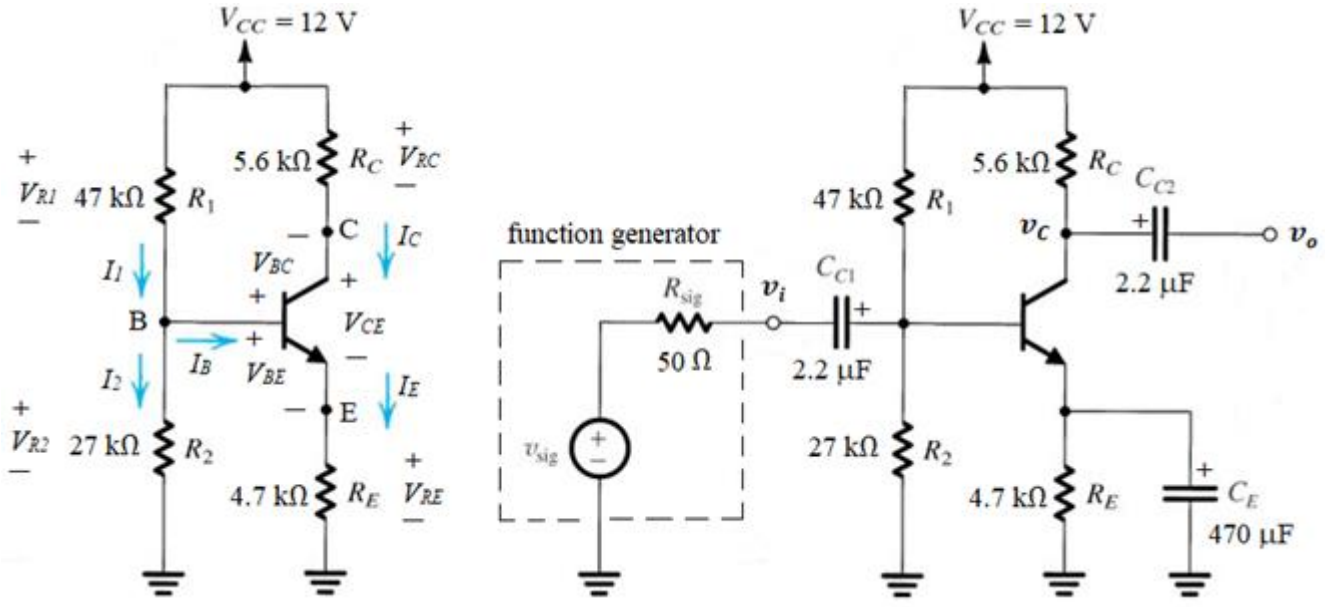
[22] At room temperature $V_T \cong 26$ mV.

PROCEDURE A: dc Measurements

1. Using a DMM, measure each resistor and record its value in Table 10.1.
2. Construct the circuit shown in Fig. 10.1a.
3. Using a DMM set to measure dc voltage, measure and record the values of V_{BE}, V_{BC}, V_{CE}, V_{R1}, V_{R2}, V_{RC} and V_{RE} on Fig. 10.2.
4. Indicate the mode of operation (cutoff, saturation or active) based on V_{BE} and V_{BC}.
5. Using the *measured* values of resistors, calculate I_C, I_E, I_1 and I_2.by Ohm's law, then record their values and direction on Fig. 10.2.
6. Using Kirchhoff's law, calculate I_B. Show its value and direction on Fig. 10.2.
7. Calculate and record $\beta = I_C / I_B$ and $\alpha = \beta/(\beta + 1)$.
8. Calculate the theoretical voltage gain A_v given by equation (10.1).

PROCEDURE B: Small Signal Measurements

1. Assemble the circuit shown in Fig 10.1b.
2. Using a signal generator, apply to your circuit a 20-$mV_{pk\text{-}pk}$, 1-kHz sinusoidal signal.
3. Display and sketch $v_i(t)$ and $v_o(t)$ on Fig. 10.3. What is the phase difference between these two signals?
4. Measure $V_{o\ (pk\text{-}pk)}$ and calculate the voltage gain: $A_v = V_{o\ (pk\text{-}pk)} / V_{i\ (pk\text{-}pk)}$.
5. Disconnect C_E, then re-measure $V_{o\ (pk\text{-}pk)}$ and calculate A_v (no need to sketch $v_o(t)$).
6. Reconnect C_E, then increase $V_{i\ (pk\text{-}pk)}$ to 500 mV; set the scope on dc coupling and 2V/DIV.
7. Display and sketch $v_c(t)$, the total collector voltage $(v_c(t) + V_C)$, on Fig. 10.4.



(a) (b)

Figure 10.1 **(a)** The CE amplifier dc bias circuit. **(b)** The complete CE amplifier circuit.

RESULTS

Table 10.1 Measured (Actual) Values of Resistors

R_C	R_E	R_1	R_2

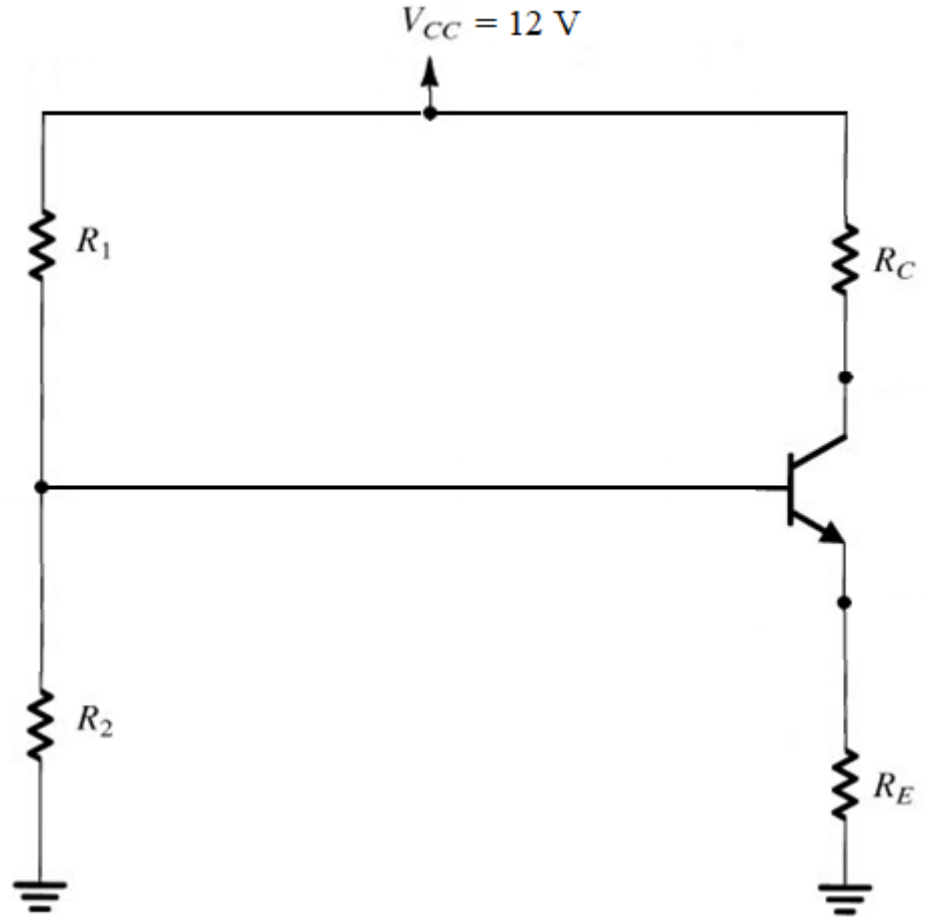


Fig. 10.2

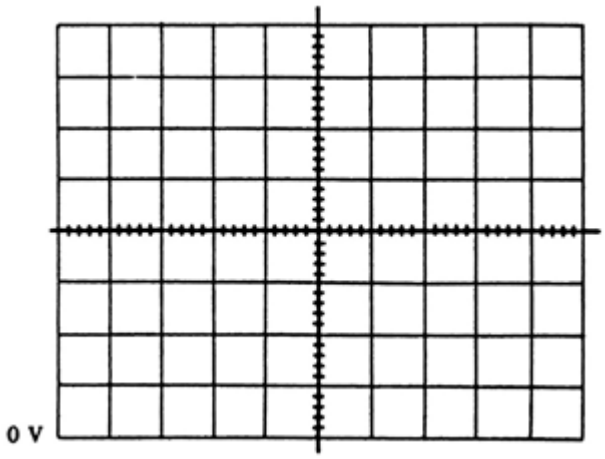


Figure 10.3

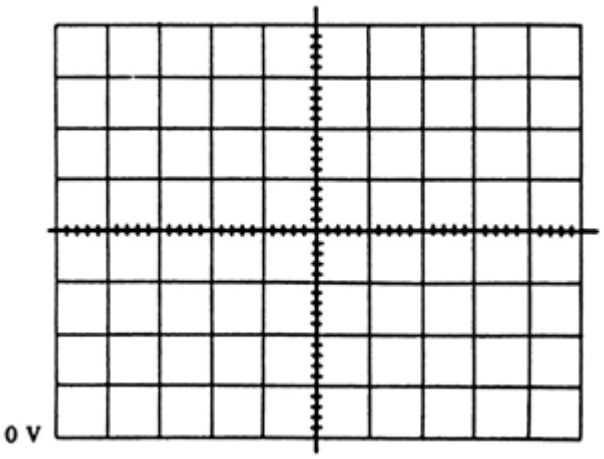


Figure 10.4

Appendix A

References

[1] A. S. Sedra and K. C.Smith, *Microelectronic Circuits*, New York: Oxford University Press, 2010.

[2] R. Boylestad and L. Nashelesky, *Electronic Devices and Circuit Theory, 7th ed.*, Upper Saddle River, NJ: Prentice-Hall Inc., 1992.

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[13] F. Mims III, *Engineer's Notebook*, Eagle Rock, Virginia: LLH Master Publishing, 1992.

Appendix B

MATLAB® Codes

(Experiment 2)

```
clf
% store voltage readings for silicon diode below
VD=[                                    ];
% store current readings for silicon diode below
ID=[                                    ];
% store voltage readings for Zener diode below
VDz=[                                   ];
% store current readings for Zener diode below
IDz=[                                   ];
plot(VD,ID,'-dk',VDz,IDz,'-*k')
axis([-6 1 -12 15])
grid on
legend('Ordinary silicon diode','Zener diode')
title({'The i-v characteristics for a an ordinary Si diode and a Zener diode';'put your name and no. here'})
% Do not forget to type you student name and number inside the above title( ) command!
xlabel('VD (V)')
ylabel('ID (mA)')
```

MATLAB® Code

(Experiment 7)

```
% plotting ID-VDS characteristics for different values of VGS for NMOS
Clf
% store your readings for VDS below
VDS=[                                   ];
% store current readings for VGS1 below
ID1=[                                    ];
% store current readings for VGS2 below
ID2=[                                    ];
% store current readings for VGS3 below
ID3=[                                    ];
figure(1)
plot(VDS,ID1,'-ob',VDS,ID2,'-dk',VDS,ID3,'-*r')
grid on
legend('VGS1 = Vt + 0.2','VGS2 = Vt + 0.3','VGS3 = Vt + 0.4')
title({'The ID-VDS characteristics for the IRF620 NMOS, Vt = ';'put your name and no. here'})
% Do not forget to type you student name and number inside the above title( ) command!
xlabel('VDS (V)')
ylabel('ID (mA)')
```

Appendix C

Datasheets

FAIRCHILD

November 2014

1N4001 - 1N4007
General-Purpose Rectifiers

Features

- Low Forward Voltage Drop
- High Surge Current Capability

DO-41
COLOR BAND DENOTES CATHODE

Ordering Information

Part Number	Top Mark	Package	Packing Method
1N4001	1N4001	DO-204AL (DO-41)	Tape and Reel
1N4002	1N4002	DO-204AL (DO-41)	Tape and Reel
1N4003	1N4003	DO-204AL (DO-41)	Tape and Reel
1N4004	1N4004	DO-204AL (DO-41)	Tape and Reel
1N4005	1N4005	DO-204AL (DO-41)	Tape and Reel
1N4006	1N4006	DO-204AL (DO-41)	Tape and Reel
1N4007	1N4007	DO-204AL (DO-41)	Tape and Reel

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value							Unit
		1N 4001	1N 4002	1N 4003	1N 4004	1N 4005	1N 4006	1N 4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current .375 " Lead Length at T_A = 75°C	1.0							A
I_{FSM}	Non-Repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
I^2t	Rating for Fusing (t < 8.3 ms)	3.7							A^2sec
T_{STG}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

Thermal Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	°C/W

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Value	Unit
V_F	Forward Voltage	I_F = 1.0 A	1.1	V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle	T_A = 75°C	30	µA
		T_A = 25°C	5.0	

Typical Performance Characteristics

Typical Performance Characteristics

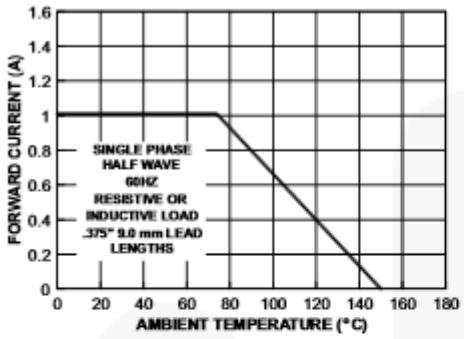


Figure 1. Forward Current Derating Curve

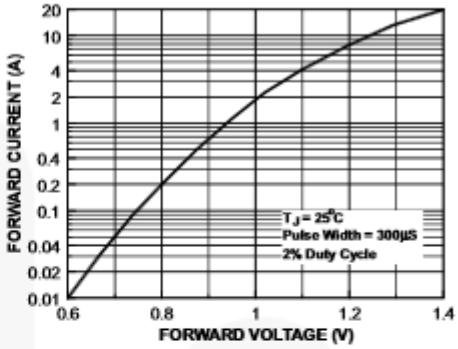


Figure 2. Forward Characteristics

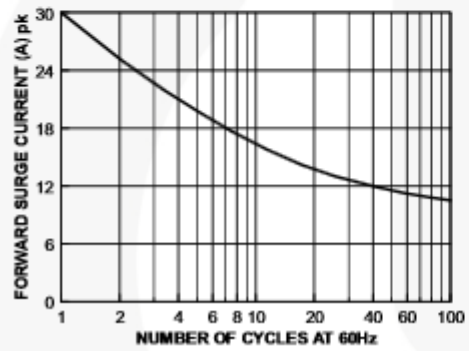


Figure 3. Non-Repetitive Surge Current

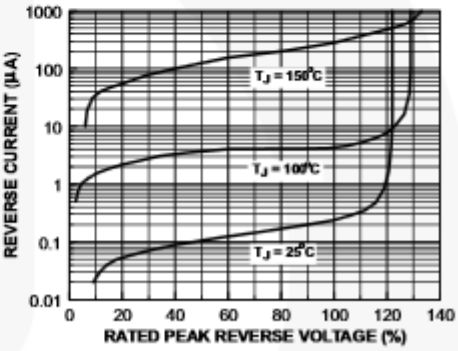


Figure 4. Reverse Characteristics

FAIRCHILD SEMICONDUCTOR®

IRF620

Data Sheet **January 2002**

5.0A, 200V, 0.800 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA9600.

Ordering Information

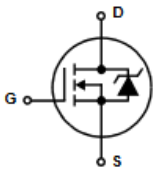
PART NUMBER	PACKAGE	BRAND
IRF620	TO-220AB	IRF620

NOTE: When ordering, use the entire part number.

Features

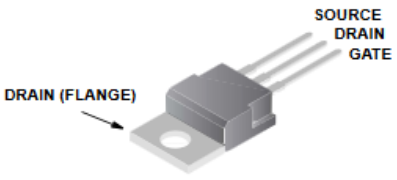
- 5.0A, 200V
- $r_{DS(ON)} = 0.800\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



IRF620

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

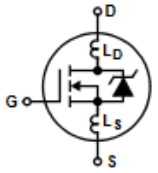
		IRF620	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	200	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	200	V
Continuous Drain Current	I_D	5.0	A
$T_C = 100^oC$	I_D	3.0	A
Pulsed Drain Current (Note 3)	I_{DM}	20	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	40	W
Linear Derating Factor		0.32	W/^{o}C
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	85	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^{o}C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^{o}C
Package Body for 10s, See TB334	T_{pkg}	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

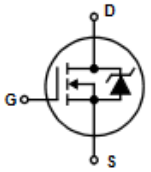
NOTE:

1. $T_J = 25^oC$ to 125^oC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA, (Figure 10)		200	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250µA		2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	25	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$		-	-	250	µA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V		5.0	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 2.5A, (Figures 8, 9)		-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, I_D = 2.5A (Figure 12)		1.3	2.5	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 100V, $I_D \approx$ 5.0A, R_G = 9.1Ω, R_L = 20Ω, MOSFET Switching Times are Essentially Independent of Operating Temperature		-	20	40	ns
Rise Time	t_r			-	30	60	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	50	100	ns
Fall Time	t_f			-	30	60	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 5.0A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)}$ = 1.5mA, (Figure 14) Gate Charge is Essentially Independent of Operating Temperature		-	11	15	nC
Gate to Source Charge	Q_{gs}			-	5.0	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	6.0	-	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz, (Figure 11)		-	450	-	pF
Output Capacitance	C_{OSS}			-	150	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	40	-	pF
Internal Drain Inductance	L_D	Measured from the Contact Screw on Tab to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	3.5	-	nH
		Measured from the Drain Lead, 6mm (0.25in) from Package to Center of Die		-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad		-	7.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.12	^{o}C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	62.5	^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier		-	-	5.0	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	20	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, I_{SD} = 5.0A, V_{GS} = 0V, (Figure 13)		-	-	1.8	V
Reverse Recovery Time	t_{rr}	$T_J = 150^oC$, I_{SD} = 5.0A, dI_{SD}/dt = 100A/µs		-	350	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^oC$, I_{SD} = 5.0A, dI_{SD}/dt = 100A/µs		-	2.3	-	µC

Typical Performance Curves Unless Otherwise Specified (Continued)

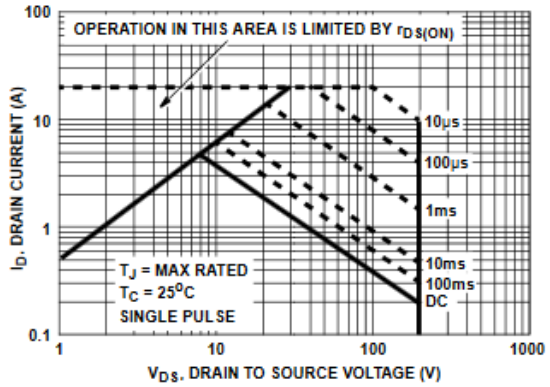


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

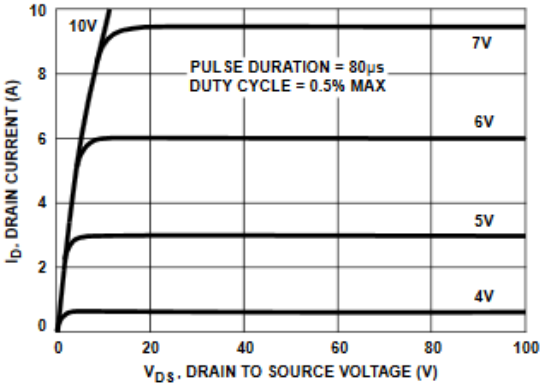


FIGURE 5. OUTPUT CHARACTERISTICS

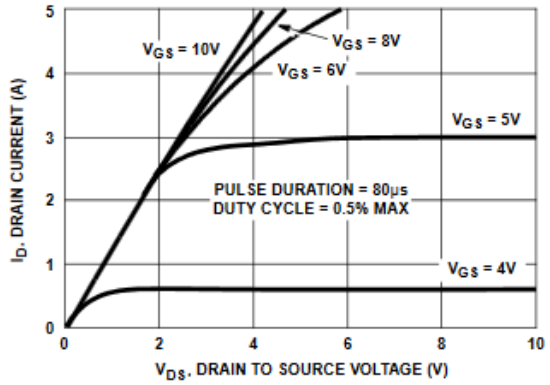


FIGURE 6. SATURATION CHARACTERISTICS

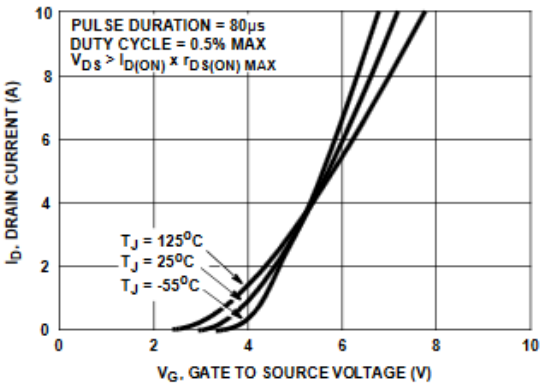
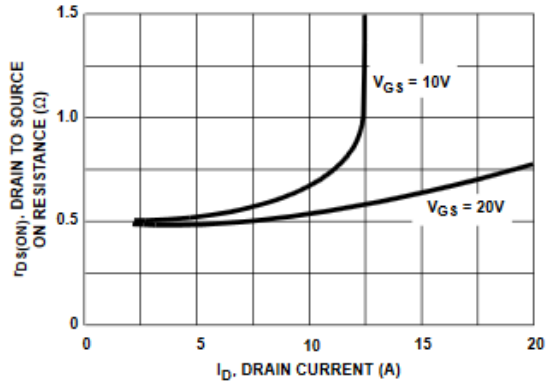


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2.0µs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

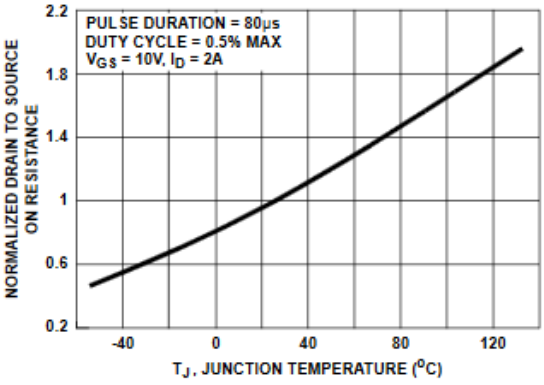


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

BD135G, BD137G, BD139G

Plastic Medium-Power Silicon NPN Transistors

This series of plastic, medium−power silicon NPN transistors are designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

Features

- High DC Current Gain
- BD 135, 137, 139 are complementary with BD 136, 138, 140
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage BD135G BD137G BD139G	V_{CEO}	 45 60 80	Vdc
Collector−Base Voltage BD135G BD137G BD139G	V_{CBO}	 45 60 100	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	1.5	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	 1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 12.5 100	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

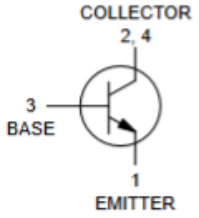
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	10	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	100	°C/W

ON Semiconductor®

http://onsemi.com

1.5 A POWER TRANSISTORS NPN SILICON 45, 60, 80 V, 12.5 W



TO−225
CASE 77−09
STYLE 1

MARKING DIAGRAM

Y = Year
WW = Work Week
BD1xx = Device Code
xx = 35, 37, 39
G = Pb−Free Package

BD135G, BD137G, BD139G

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector−Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0) BD135G BD137G BD139G	BV_{CEO}*	 45 60 80	 – – –	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125°C)	I_{CBO}	 – –	 0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	10	μAdc
DC Current Gain (I_C = 0.005 A, V_{CE} = 2 V) (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A V_{CE} = 2 V)	h_{FE}*	 25 40 25	 – 250 –	–
Collector−Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*	 –	 0.5	Vdc
Base−Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*	 –	 1	Vdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

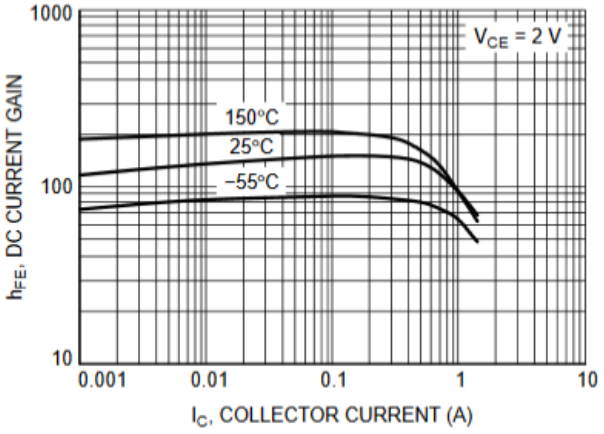


Figure 1. DC Current Gain

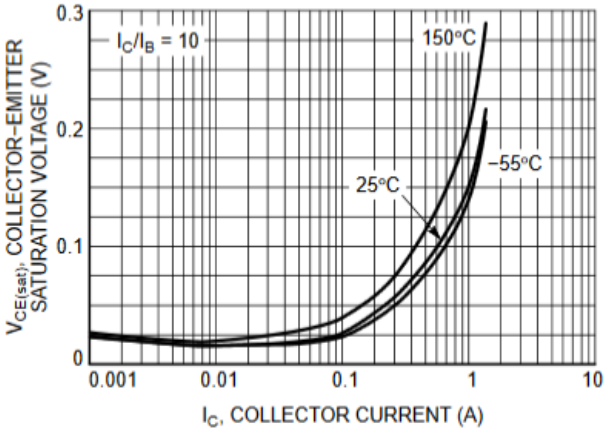


Figure 2. Collector−Emitter Saturation Voltage

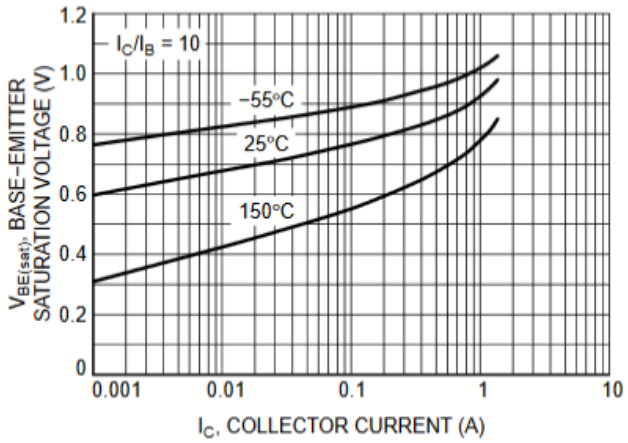


Figure 3. Base−Emitter Saturation Voltage

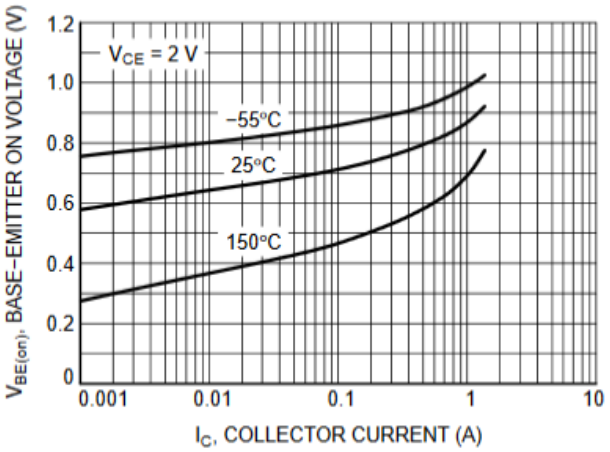


Figure 4. Base−Emitter On Voltage

Appendix D

Type	Part Number	Ratings	Type	Part Number	Ratings
Rectifier Diode	1N1183	50V 35A	Rectifier Diode	1N4001	50V 1A
Rectifier Diode	1N1184	100V 35A	Rectifier Diode	1N4002	100V 1A
Rectifier Diode	1N1186	200V 35A	Rectifier Diode	1N4003	200V 1A
Rectifier Diode	1N1187	300V 35A	Rectifier Diode	1N4004	400V 1A
Rectifier Diode	1N1199	50V 35A	Rectifier Diode	1S310	50V 0.5A
Rectifier Diode	1N3910	100V 30A	Rectifier Diode	1S311	100V 0.5A
Rectifier Diode	1N3911	200V 30A	Rectifier Diode	ERA3804	400V 0 .5A
Rectifier Diode	1N3491	50V 25A	Switching Diode	1N4500	80V 500mA
Rectifier Diode	1N3492	100V 25A	Switching Diode	BA220	10V 400mA
Rectifier Diode	1N3493	200V 25A	Switching Diode	BAS45	125V 225mA
Rectifier Diode	1N3494	300V 25A	Switching Diode	1N916	100V 200mA
Rectifier Diode	1N3900	100V 20A	Switching Diode	1N3600	75V 200mA
Rectifier Diode	1N3901	200V 20A	Switching Diode	1N4148	75V 200mA
Rectifier Diode	MUR1610CT	100V 16A	Switching Diode	1N4450	40V 200mA
Rectifier Diode	MUR1620CT	200V 16A	Switching Diode	1N4152	40V 200mA
Rectifier Diode	1N1200	100V 12A	Switching Diode	1N4154	35V 200mA
Rectifier Diode	1N1202	200V 12A	Switching Diode	1N4534	75V 150mA
Rectifier Diode	1N1204	400V 12A	Switching Diode	1N4531	100V 125mA
Rectifier Diode	MUR805	50V 8A	Switching Diode	1N4532	75V 125mA
Rectifier Diode	MUR810	100V 8A	Switching Diode	1N3064	75V 75mA
Rectifier Diode	MBR1535CT	35V 7.5A	Varactor Diode	1N5443	30V 10pf
Rectifier Diode	1N3879	50V 6A	Varactor Diode	1N5449	30V 27pf
Rectifier Diode	1N3880	100V 6A	Varactor Diode	1N5453	30V 56pf
Rectifier Diode	1N3881	200V 6A	Varactor Diode	1N5456	30V 100pf
Rectifier Diode	1N3882	300V 6A	Varactor Diode	BB112	12V 470p
Rectifier Diode	MUR405	50V 4A	Schottky Diode	10KQ100	100V 10A
Rectifier Diode	MUR410	100V 4A	Schottky Diode	10KQ30	30V 10A
Rectifier Diode	MUR420	200V 4A	Schottky Diode	5KQ60	60V 5A
Rectifier Diode	1N4719	50V 3A	Schottky Diode	5KQ90	90V 5A
Rectifier Diode	1N4720	100V 3A	Schottky Diode	1N5821	30V 3A
Rectifier Diode	1N4721	200V 3A	Schottky Diode	1N5822	40V 3A
Rectifier Diode	1N5400	50V 3A	Schottky Diode	ERB83006	60V 2A
Rectifier Diode	1N5401	100V 3A	Schottky Diode	ERB84009	90V 2A
Rectifier Diode	1N5402	200V 3A	Schottky Diode	ERA83006	60V 1A
Rectifier Diode	BY296	100V 2A	Schottky Diode	ERA85009	90V 1A
Rectifier Diode	BY297	200V 2A	Diode Bridges	MDA2502	200V 25A, Full Wave
Rectifier Diode	BYV27-50	50V 2A	Diode Bridges	MDA2504	400V 25A, Full Wave
Rectifier Diode	BYV27-100	100V 2A	Diode Bridges	KBPC801	80V 8A, Full Wave
Rectifier Diode	1N5391	50V 1.5A	Diode Bridges	KBPC804	250V 8A, Full Wave
Rectifier Diode	1N5392	100V 1.5A	Diode Bridges	KBU4D	200V 4A, Full Wave
Rectifier Diode	1R5BZ41	100V 1.5A	Diode Bridges	KBU4G	400V 4A, Full Wave
Rectifier Diode	1N5393	200V 1.5A	Diode Bridges	KBU4J	600V 4A, Full Wave

Appendix E

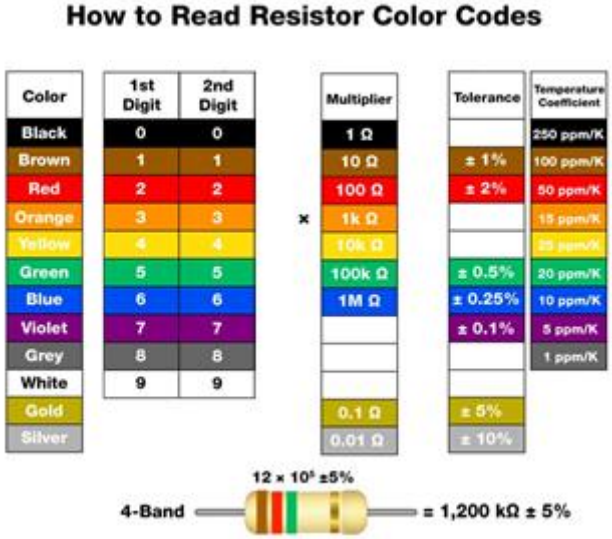
ZENER DIODE TABLE								
Volt	0.4 Watt		0.5 Watt		1 Watt		5 Watt	
2.4			1N5221	1N4617		UZ87=UZ88		UZ51=52=53
2.5			1N5222			UZ81=UZ82		UZ57=58=59
2.7			1N5223	1N4618				
2.8			1N5224					
3.0			1N5225	1N4619				
3.3	1N746		1N5226	1N4620	1N4728		1N5333	
3.6	1N747		1N5227	1N4621	1N4729		1N5334	
3.9	1N748		1N5228	1N4622	1N4730		1N5335	
4.3	1N749		1N5229	1N4623	1N4731		1N5336	
4.7	1N750		1N5230	1N4624	1N4732		1N5337	
5.1	1N751		1N5231	1N4625	1N4733		1N5338	
5.6	1N752		1N5232	1N4626	1N4734		1N5339	
6.0			1N5233	1N469			1N5340	
6.2	1N753		1N5234	1N4627	1N4735		1N5341	
6.8	1N754	1N957	1N5235	1N4628	1N4736	UZ8806	1N5342	UZ5806
7.5	1N755	1N958	1N5236	1N4629	1N4737	UZ8807	1N5343	UZ5807
8.2	1N756	1N959	1N5237	1N4630	1N4738	UZ8808	1N5344	UZ5808
8.7			1N5238	1N4695			1N5345	
9.1	1N757	1N960	1N5239	1N4631	1N4739	UZ8809	1N5346	UZ5809
10.0	1N758	1N961	1N5240	1N4632	1N4740	UZ8810	1N5347	UZ5810
11.0		1N962	1N5241	1N4633	1N4741		1N5348	
12.0	1N759	1N963	1N5242	1N4634	1N4742	UZ8812	1N5349	UZ5812
13.0	1N717	1N964	1N5243	1N4635	1N4743	UZ8813	1N5350	UZ5813
14.0			1N5244				1N5351	UZ5814
15.0	1N718	1N965	1N5245	1N4636	1N4744	UZ8815	1N5352	UZ5815
16.0	1N719	1N966	1N5246	1N4637	1N4745	UZ8816	1N5353	UZ5816
17.0			1N5247				1N5354	
18.0	1N720	1N967	1N5248	1N4638	1N4746	UZ8818	1N5355	UZ5818
19.0			1N5249				1N5356	
20.0	1N721	1N968	1N5250	1N4639	1N4747	UZ8820	1N5357	UZ5820
22.0	1N722	1N969	1N5251	1N4640	1N4748	UZ8822	1N5358	UZ5822
24.0	1N723	1N970	1N5252	1N4641	1N4749	UZ8824	1N5359	UZ5824
25.0			1N5253				1N5360	
27.0	1N724	1N971	1N5254	1N4642	1N4750	UZ8827	1N5361	UZ5827
28.0			1N5255				1N5362	
30.0	1N725	1N972	1N5256	1N4643	1N4751	UZ8830	1N5363	UZ5830
33.0	1N726	1N973	1N5257	1N4644	1N4752	UZ8833	1N5364	UZ5833
36.0	1N727	1N974	1N5258	1N4645	1N4753	UZ8836	1N5365	UZ5836
39.0	1N728	1N975	1N5259	1N4646	1N4754	UZ8840	1N5366	UZ5840
43.0	1N729	1N976	1N5260	1N4647	1N4755		1N5367	
47.0	1N730	1N977	1N5261	1N4648	1N4756	UZ8845	1N5368	
51.0	1N731	1N978	1N5262		1N4757	UZ8850	1N5369	UZ5850
56.0	1N732	1N979	1N5263		1N4758	UZ8856	1N5370	UZ5856
60.0			1N5264				1N5371	UZ5860
62.0	1N733	1N980	1N5265		1N4759	UZ8860	1N5372	
68.0	1N734	1N981	1N5266		1N4760	UZ8870	1N5373	
75.0	1N735	1N982	1N5267		1N4761	UZ8875	1N5374	UZ5875
82.0	1N736	1N983	1N5268		1N4762	UZ8880	1N5375	UZ5880
87.0			1N5269				1N5376	
91.0	1N737	1N984	1N5270		1N4763	UZ8890	1N5377	UZ5890
100.0	1N738	1N985	1N5271		1N4764	UZ8110	1N5378	UZ5310
110.0	1N739	1N986	1N5272			UZ8111	1N5379	UZ5311
120.0	1N740	1N987	1N5273			UZ8112	1N5380	UZ5312
130.0	1N741	1N988	1N5274			UZ8113	1N5381	UZ5313
140.0			1N5275			UZ8114	1N5382	UZ5314
150.0	1N742	1N989	1N5276			UZ8115	1N5383	UZ5315
160.0	1N743	1N990	1N5277			UZ8116	1N5384	UZ5316
170.0			1N5278			UZ8117	1N5385	UZ5317
180.0	1N744	1N991	1N5279			UZ8118	1N5386	UZ5318
190.0			1N5280			UZ8119	1N5387	UZ5319
200.0	1N745	1N992	1N5281			UZ8120	1N5388	UZ5320

Appendix F

Standard Components Values

Resistors

Standard Resistor Values (±5%)						
1.0	10	100	1.0 k	10 k	100 k	1.0 M
1.1	11	110	1.1 k	11 k	110 k	1.1 M
1.2	12	120	1.2 k	12 k	120 k	1.2 M
1.3	13	130	1.3 k	13 k	130 k	1.3 M
1.5	15	150	1.5 k	15 k	150 k	1.5 M
1.6	16	160	1.6 k	16 k	160 k	1.6M
1.8	18	180	1.8 k	18 k	180 k	1.8 M
2.0	20	200	2.0 k	20 k	200 k	2.0 M
2.2	22	220	2.2 k	22 k	220 k	2.2 M
2.4	24	240	2.4 k	24 k	240 k	2.4 M
2.7	27	270	2.7 k	27 k	270 k	2.7 M
3.0	30	300	3.0 k	30 k	300 k	3.0 M
3.3	33	330	3.3 k	33 k	333 k	3.0 M
3.6	36	360	3.6 k	36 k	360 k	3.6 M
3.9	39	390	3.9 k	39 k	390 k	3.9 M
4.3	43	430	4.3k	43 k	430 k	4.3 M
4.7	47	470	4.7 k	47 k	470 k	4.7 M
5.1	51	510	5.1 k	51 k	510 k	5.1 M
5.6	56	560	5.6 k	56 k	560 k	5.6 M
6.2	62	620	6.2 k	62 k	620 k	6.2 M
6.8	68	680	6.8 k	68 k	680 k	6.8 M
7.5	75	750	7.5 k	75 k	750 k	7.5 M
8.2	82	820	8.2 k	82 k	820 k	8.2 M
9.1	91	910	9.1 k	91 k	910 k	9.1 M



Standard Components Values

Electrolytic Capacitors

0.1 µF	68 µF	480 µF	3900 µF	30,000 µF
0.15 µF	72 µF	500 µF	4000 µF	31,000 µF
0.22 µF	75 µF	510 µF	4100 µF	32,000 µF
0.33 µF	82 µF	520 µF	4200 µF	33,000 µF
0.47 µF	88 µF	540 µF	4300 µF	34,000 µF
0.68 µF	100 µF	550 µF	4600 µF	36,000 µF
1 µF	108 µF	560 µF	4700 µF	37,000 µF
1.5 µF	120 µF	590 µF	4800 µF	38,000 µF
2 µF	124 µF	620 µF	5000 µF	39,000 µF
2.2 µF	130 µF	645 µF	5100 µF	40,000 µF
3 µF	140 µF	650 µF	5400 µF	41,000 µF
3.3 µF	145 µF	680 µF	5500 µF	47,000 µF
4 µF	150 µF	700 µF	5600 µF	48,000 µF
4.7 µF	161 µF	708 µF	5800 µF	50,000 µF
5 µF	170 µF	730 µF	6000 µF	55,000 µF
5.6 µF	180 µF	800 µF	6500 µF	56,000 µF
6.8 µF	189 µF	820 µF	6800 µF	60,000 µF
7 µF	200 µF	850 µF	7200 µF	62,000 µF
8 µF	210 µF	860 µF	7400 µF	66,000 µF
8.2 µF	216 µF	1000 µF	7600 µF	68,000 µF
10 µF	220 µF	1100 µF	7800 µF	76,000 µF
12 µF	230 µF	1200 µF	8200 µF	0.1 F
15 µF	233 µF	1300 µF	8300 µF	0.11 F
16 µF	240 µF	1400 µF	8400 µF	0.12 F
18 µF	243 µF	1500 µF	8700 µF	0.15 F
20 µF	250 µF	1600 µF	9000 µF	0.22 F
21 µF	270 µF	1700 µF	9600 µF	0.33 F
22 µF	300 µF	1800 µF	10,000 µF	0.47 F
24 µF	320 µF	2000 µF	11,000 µF	0.666 F
25 µF	324 µF	2100 µF	12,000 µF	
27 µF	330 µF	2200 µF	13,000 µF	
30 µF	340 µF	2500 µF	15,000 µF	
33 µF	350 µF	2600 µF	16,000 µF	
35 µF	370 µF	2700 µF	17,000 µF	
36 µF	378 µF	2800 µF	18,000 µF	
39 µF	380 µF	2900 µF	20,000 µF	
40 µF	390 µF	3000 µF	22,000 µF	
43 µF	400 µF	3100 µF	23,000 µF	
47 µF	420 µF	3300 µF	24,000 µF	
50 µF	430 µF	3400 µF	25,000 µF	
53 µF	450 µF	3500 µF	26,000 µF	
56 µF	460 µF	3600 µF	27,000 µF	
60 µF	470 µF	3700 µF	28,000 µF	